Paweł Śniatała

Summary of professional accomplishment

Poznań, 2016

Contents

Poznań, 29.01.2016 r.

1. First and last name:
   Paweł Śniatała

2. **Education and scientific degrees:**
   - **MSc in telecommunication:** Poznan University of Technology, Faculty of Electrical Engineering, 1988r.
   - **MSc in computer science:** Poznan University of Technology, Faculty of Electrical Engineering, 1990r.
   - **PhD degree in microelectronics**, 1996. PhD thesis: ”Settling time in analog discrete time circuits”; supervisor: prof. dr hab. inż. Andrzej Handkiewicz, reviewers: prof. dr hab. inż. Andrzej Napieralski (Łódź University of Technology), prof. dr hab. inż. Marek Domański (Poznan University of Technology).
   - **Master of Business Administration** Georgia State University, Atlanta, USA /Poznań Univeristy of Economics, 2004.

3. **Employment in academic institutions**

2017 – present
Assistant professor (pol. Adiunkt)
Poznan University of Technology, Faculty of Computing,
Institute of Computing Science (http://www2.cs.put.poznan.pl/en/)

2016
Habilitation degree in Electronics, Łódź University of Technology
Poznan University of Technology, Faculty of Computing,
Department of Computer Engineering

2002 – 2011
Assistant professor (pol. Adiunkt)
Poznan University of Technology, Faculty of Computing,
Department of Computer Engineering

2000 - 2002,
Assistant Professor, tenure track position,
Rochester Institute of Technology, Department of Computer Engineering,
Rochester, NY USA

1998 - 2002,
Visiting Assistant Professor/ Tenure Track Assistant Professor
Rochester Institute of Technology, Department of Computer Engineering,
Rochester, NY USA

1996-1998
Assistant professor (pol. Adiunkt)
Poznan University of Technology, Faculty of Computing,
Department of Computer Engineering
1990-1996,
Assistant
Poznan University of Technology, Faculty of Computing,
Department of Computer Engineering
1988-1997
IT manager
Poznan University of Medical Science

4. The main publication, which presents the author's research results in the topic of the **ΣΔ Modulators** is a monograph:

„CMOS Current Mode ΣΔ Modulators"

published in series "Poznan Monographs in Computing and Its Applications", editor-in-chief: prof. Jan Węglarz, Poznan University of Technology & Poznan Supercomputing and Networking Center. Publisher NAKOM, Poznań 2016 (158 pages in English).

a) Other publications related to this topic:

[Sniatala04]
Śniatała P., Botha A.S., „A/D converter based on a new memory cell implemented using the switched current technique", Microelectronics Reliability vol.44, 2004, pp.861-867.

[Sniatala15c]
Śniatała P., Handkiewicz A., Szczęsny S., Naumowicz M., Melo J., Paulino N., Goes J., "Current mode sigma-delta modulator designed with the help of transistor's size optimization tool", Bulletin of the Polish Academy of Sciences, Technical Sciences, Vol. 63, No. 4, 2015. DOI: 10.1515/bpasts-2015-0104 .

[Sniatala12]
Handkiewicz A., Katarzyński P., Szczęsny S., Wencel J., **Śniatała P**. ; "Analog filter pair design on the basis of a gyrator–capacitor prototype circuit", International Journal of Circuit Theory and Applications, 2012, vol.40, no.6, pp.539-550.

[Sniatala14]
Handkiewicz A., Katarzyński P., Szczęsny S., Naumowicz M, Melosik M., **Śniatała P.**, "VHDL-AMS in SI (switched-current) analog filter pair design based on a gyrator-capacitor prototype circuit", International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, DOI: 10.1002/jnm.1921, Vol.27, pp.268-281, March 2014.

[Sniatala14a]
Handkiewicz A., Katarzyński P., Szczęsny S., Naumowicz M., Melosik M., **Śniatała P.**, Kropidłowski M., "Design automation of a lossless multiport network and its application to image filtering", Expert Systems With Applications, pp.2211-2221, vol 41, Issue 5, 2014 ISSN 0957-4175.

[Sniatala15]
Handkiewicz A., Szczęsny S., Naumowicz M., Katarzyński P., Melosik M., **Śniatała P.**, Kropidłowski M., "SI-Studio, a layout generator of current mode circuits", Expert Systems With Applications, 2015/4/15, vol.42, no.6 , pp.3205-3218.

[Sniatala05]
Śniatała P., "VHDL-AMS Descriptions to Accelerate Analog SI Circuits Design", IEEJ International Analog VLSI Workshop, Bordeaux 2005, AVLSIW, No. 47.

[Sniatala06]
Śniatała P., Rudnicki R., "Automated Design and Layout Generation for Switched Current Circuits", Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS 2006), pp. 637-640, ISBN: 0-7803-9390-2.

4.1. Introduction

The continuous development of integrated circuits production technologies led to the reduction of transistors' sizes to the level of several dozen nanometers. According to the International Technology Roadmap for Semiconductors (ITRS) [1], the miniaturization of circuits by scaling down the transistor has been the principal driver for the semiconductor technology roadmap, for many years. This direction for further progress is labeled "More Moore" in Fig. 1.1. The second trend is characterized by functional diversification of semiconductor-based devices. The non-digital functionalities do contribute to the miniaturization of electronic systems. Consequently, in view of added functionality, this trend may be designated "More-than-Moore" (MtM), as depicted in Fig. 1.1. The MtM approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board level into a particular package level (System-in-Package) or chip-level (System-on-a-Chip) potential solution. The world around us is an analog world, full of information useful to our civilization. We measure just about everything imaginable via sensors and convert the data into digital signals utilizing analog-to-digital converters (ADCs). In most cases, the output from sensors requires additional preprocessing to provide the best possible signal to the ADC.
As the feature size of CMOS processes decreases, the supply voltage has to be reduced to ensure the reduction of power dissipation per cell. However, the reduction in supply voltage leads to degradation of circuit performance in terms of available bandwidth and voltage swing. Scaling down the threshold voltage of the MOSFETs reduces the performance loss

(degraded bandwidth, low voltage swing etc.) to some extent but it has its own disadvantages i.e. the increase in the static power dissipation. The performance of digital circuits is improved by scaling but the analog cells benefit marginally because minimum size transistors cannot be used due to noise and offset requirements. Current mode circuits are a possible solution for the low voltage high performance analog circuit since they offer voltage-independent high bandwidth. In current mode circuits (CMCs) the complete circuit response is determined by the currents and the input/output signals are primarily currents. The voltage levels are irrelevant in determining the circuit performance. CMCs have simple architecture and their operations do not depend on the supply voltages. Analog circuits should have rail-to-rail input and output voltage swing capability for high Signal-to-Noise Ratio (SNR), which can be obtained using the CMCs.
As a result of lowering feature size of CMOS technology, analog circuits fabricated in nanotechnologies suffer from many nonidealities, which cause lower accuracy of analog blocks. One of the possible approaches to reduce this effect is to use low sensitive structures of the design systems. In the area of A/D converters, a structure which does not require accurate elements is the ΣΔ modulator. Such circuits can offer reasonable speed and resolution parameters without necessity of using high accuracy components. It leads to the use of sigma-delta analog-to-digital converters in a wide range of applications. Connecting the idea of the ΣΔ modulation with the current mode circuits seems to be an interesting solution, which is the author's area of research work.

The monograph „CMOS Current Mode ΣΔ Modulators", presents author's research results in the area of current mode ΣΔ modulators implementations. Chapter 2 introduces the principle of the oversampling and noise shaping techniques as well as the qualitative parameters of the modulators. In particular, Walden's Figure-of-Merit (FoM) was used throughout the book to compare different realizations of modulators. This FoM relates the ADC power dissipation to its performance, represented by the sampling rate and conversion error amplitude.
The rest chapters (3,4,5,6) present original author's results, which are summarized below.

4.2. VHDL-AMS behavioral models of chosen modulator's blocks

There are several reasons for using higher level analog modeling (functional, behavioral or macro-modeling) for describing and simulation of mixed-signal systems, which are cited after Gielen and Rutenbar [32, 33]:

- The simulation time of circuits with widely spaced time constants (e.g., oversampling converters) is quite large since the time-step control mechanism of the analog solver follows the fastest signal in the circuits. Use of higher-level modeling for the blocks will accelerate the simulation of these systems.
- In a top-down design methodology at higher levels, there is a need for higher-level models to describe the pin-to-pin, since the details of the underlying circuit implementation are simply not yet known and hence only generic mathematical models can be used.
- Behavioral models can be used in the bottom-up system verification ; it reduces the CPU time required to simulate a block as a part of a larger system.

- When providing or using analog IP macro-cells in a system-on-chip context, a virtual component has to be accompanied by an executable model that efficiently models the pin-to-pin behavior of this virtual component. This model can be used by the SoC integrating company, even without knowing the detailed circuit implementation of the macro-cell.

Chapter 3 of the monograph presents VHDL-AMS behavioral models of basic modules of the ΣΔ modulators. The development of new electronic technologies allows us to increase of the complexity of modern System on Chip (SoC) devices. These devices contain a complete analog and digital processing chain. High level simulations, based on behavioral models, are very helpful for initial verification of mixed-signal systems. There are many computer tools/languages, which can be used for this purpose, e.g., MATLAB, SCILAB, Verliog-AMS, VHDL-AMS. ΣΔ modulators, discussed in this work, are usually implemented as a part of A/D converters and provide interfaces between analog sensors and digital processing of the measured values. The sensors can measure different parameters like temperature, pressure, pH etc. Consequently, we can say that the circuits work not only at the border between analog and digital representation in the electrical domain but also often between other domains like temperature, pressure, flow, pH and/or many other non-electrical domains. The models of these nonelectrical blocks are also required in order to be able to simulate the whole system. It is where the HDL-AMS languages fit perfectly.

The elaborated VHDL-AMS library of basic models includes the following primitives: sample and hold, SI memory cell, delay element, integrator (bilinear, Euler forward, Euler backward), one bit D/A converter (current output), A/D converter (current input), digital decimation filter (for testbench structure), digital register (for testbench structure). The models are parameterized, which allows us to simulate different scenarios and to find optimal parameters. These parameters, in VHDLAMS represented as generics, can be used as goal functions during the transistor dimensions optimization process for the given technology. Another important feature which was assumed in the model design is the interface. A model's interface needs to have the same terminals as a SPICE model in order to allow straightforward exchange them with the transistor level description. In other words, they should be described in the time domain, having input/output currents and voltages matching their real, transistor level counterparts. Most of the presented in the monographs examples are pure behavioral models. However, a model in current/voltage domain of an example 1-st order ΣΔ modulator is also presented. The designed VHDL-AMS models were used to simulate the whole A/D converter. A testbench created to test different ΣΔ modulator structures is presented in Fig. 1. The elaborated VHDL-AMS code was validated by comparison to the results of the theoretical equation (calculation of SNDR parameter) and by comparison to the transistor level simulations as well. It has proved the efficiency and accuracy of the elaborated models.

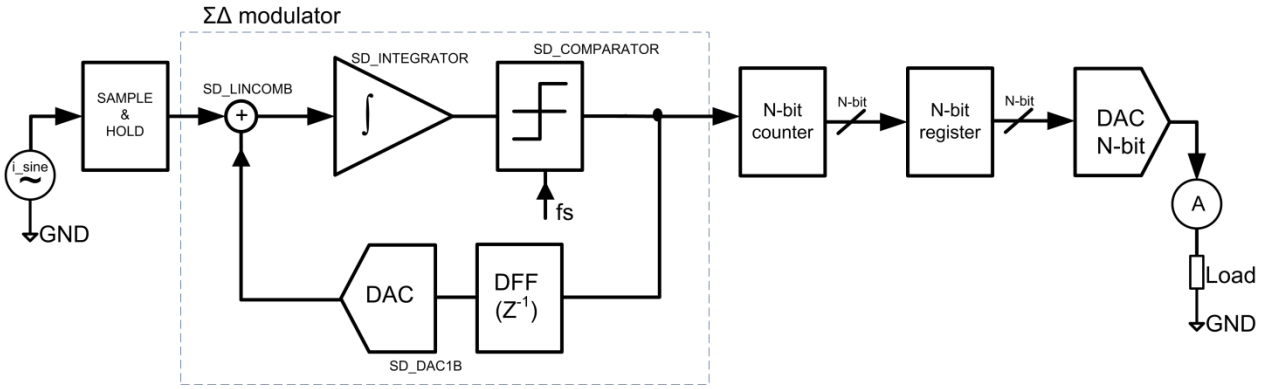

Fig. 1. *A/D converter testbench with elaborated VHDL-AMS models.*

VHDL-AMS descriptions of analog circuits, proposed by author in [Sniatala04] were also used in elaborated CAE tools for filters, filter pairs, and bank of filters design. The results of this research were presented also in author's publications [Sniatala12] and [Sniatala14a].

4.3. Continuous time, current mode ΣΔ modulator structures.

Chapter 4 of the monograph presents current mode continuous time ΣΔ modulators. The first section introduces the basic element of the modulator, which is a loop filter. The filter is implemented as a continuous time current mode integrator based on the current mirror. First, the basic structure of the integrator is analyzed; next, its fully differential implementation is introduced. Based on both integrator structures, second order ΣΔ modulators are designed. The first modulator is implemented using the basic version of the integrator. Its structure is presented in *Fig. 2*.

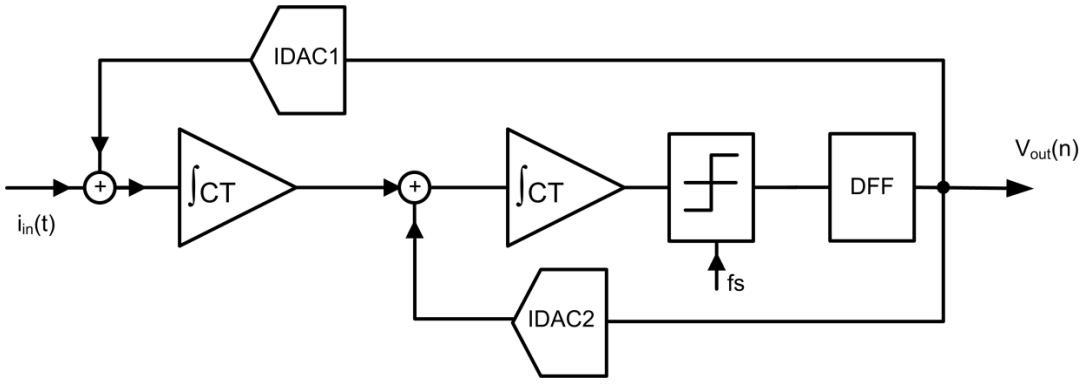

Fig. 2 Second order ΣΔ modulator structure.

The modulator consists of two current mode integrators, a current comparator, a flip-flop and a DAC with a current output. The integrator is built based on a simple current mirror with an additional capacitance added to the gates. The current comparator applied in the

modulator is a structure composed of a diode connected CMOS pair followed by inverters. The first pair of transistors acts as a current-to-voltage converter. Next, the following inverters act as voltage amplifiers. Another tool was elaborated to optimize the comparator transistors' dimensions. The program is based on the Hooke-Jeeves pattern search method. More details about this implementation were presented in [Sniatala15c]. The SNDR parameter of the modulator designed for TSMC 65 nm was SNDR=53.6 dB. The Figure-of_Merit was FoM=59.7 fJ/conv.

In order to further optimize the structure, we proposed a novel, hybrid solution. In this solution, presented in *Fig. 3*, we combine the continuous time current-mode technique and a passive filter topology. We achieved a dynamic range of 65 dB and SNDR peaks of 60.7 dB. The total power dissipation with a 1.1 V power supply is 132 µW. The FoM is 37.3 fJ/conv for a 2 MHz bandwidth. This current-mode active-passive continuous time ΣΔ modulator demonstrated that it is possible to obtain a good compromise between power consumption and performance of an ADC. We completed the presentation of continuous time modulators implemented in a MASH-2-2 structure, which is described in monograph in Section 4.4.

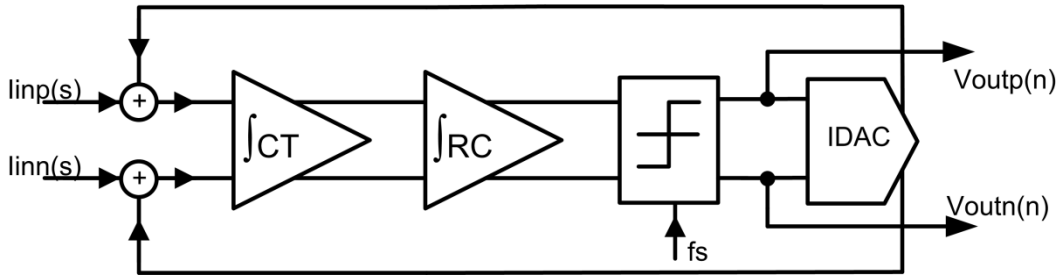

Fig. 3 Hybrid, active-passive modulator structure.

4.4. Switched current (SI) technique, SI ΣΔ modulator implementations.

Chapter 5 is devoted to switched-current circuits. Author introduced a new idea of a memory cell. Based on this new cell, new circuits were designed and tested: a delay cell, a bilinear, fully differential integrator, and finally the whole ΣΔ modulator. One section was dedicated to the current mode comparators, which were applied in the modulators. The presented circuits were implemented in different technologies, namely AMS CY E 0.8 µm, AMS 0.35 µm and TSMC 0.18 µm. The layouts were created with the help of different tools. The first implementation was prepared using the Compass tool; next, Mentor Graphics and Cadence were used.

4.5. Modeling, simulation and CAE tools.

Chapter 6 presents new computer tools devised to improve the design process at different levels. We prepared the AMS2SI tool to automate the translation process from the VHDL-AMS modulator description at the architecture level to more specific descriptions at the circuit and/or device levels. The resulting files contain VHDL-AMS code and/or SPICE netlist

for a particular technique and technology. We used the elaborated tool to design the switched-current ΣΔ modulator fabricated in the 0.18 µm, single poly, six metal, silicide MOS process. This circuit was presented in Chapter 5. Optimization programs, dedicated to the designed current mode circuits, were also described. Finally, with reference to the layout level, we devised the Automation Layout Generator (ALG) program. This tool is prepared using the AMPLE language and it considerably speeds up the laborious layout drawing. The second part of Chapter 6 presents testing environments dedicated to the fabricated chips. Thanks to the introduction of programmable devices (CPLD, FPGA) we simplified the measurement procedures. As a result, we were able to easily generate the required control and testing signals. The example measurements screen-shots are included in this chapter.

5. **Other scientific achievements**

The other author's research activity includes image processing and in general mixed analog-digital processing. Especially it is worth to mention about author's works related to hardware implementation of image processing. Author was a principal investigator of the grant "Web Based VHDL library for Multimedia Processing Algorithms" and a prime contractor of the grant "Hardware Implementation of Document Image Processing Algorithm" (both funded by the National Science Foundation through Rochester Institute of Technology, USA). Author elaborated algorithms of MPEG-7 descriptions extraction. The following descriptors were implemented: scalable color descriptor, color layout descriptor, color structure descriptor, motion activity descriptor. The algorithms were implemented not only in software but in hardware as well. The circuits were synthesized based on different hardware description languages. In particular effectiveness of synthesis based on VHDL and Handel-C were compared. The elaborated structures were implemented on RC1000 Celoxica board, which includes FPGA Xilinx Virtex V1000. ASIC versions of the circuits were also designed for AMS 0.35µm C35B4 technology. These research results were published in the papers listed below.

Continuing the image processing topic, author currently is participating in NCBIR grant "Intelligent system for pavement condition monitoring". Author is responsible for design and implementation of computer tools dedicated to automation pavement crack detection based on road's pictures. The first results were published in [Sniatala15b].

[Sniatala11]
Kapela R., **Śniatała P.**, Rybarczyk A.,"Real-time Visual Content Description System based on MPEG-7 descriptors", Multimedia Tools and Applications, vol. 53, no. 1, pp. 119-150, 2011.

[Sniatala15a]
Kapela R., Gugała K., **Śniatała P.**, Świetlicka A., Kolanowski K., "Embedded Platform for Local Image Descriptor Based Object Detection", Applied Mathematics and Computation, vol. 267, pp.419-426, 2015.

[Sniatala15b]
Kapela R., **Śniatała P.,** Turkot A., Pożarycki A., Wyczałek M., Błoch A., Rybarczyk A., „Asphalt surfaced pavement cracks detection based on Histograms of Oriented Gradients", ", Proc. 21th Mixed Design of Integrated Circuits and Systems, MIXDES'2015.

[Sniatala07a]
Śniatała P., Kapela R., Rudnicki R., Rybarczyk A."Efficient Hardware Architecture of Selected MPEG-7 Color Descriptors"., Proceedings of 15th European Signal Processing Conference, EUSIPCO 2007.

[Sniatala04a]
Śniatała P., Savakis A., Rudnicki R.: „FPGA based system for MPEG-7 Descriptors Extraction", Proc. 11th International Workshop on Systems, Signals and Image Processing, IWSSIP'2004, Poznań, pp. 171-174.

[Sniatala04b]
Śniatała P., Rudnicki R., Savakis A.: „Hardware Implementation of MPEG-7 Color Descriptors", Proc. 11th Mixed Design of Integrated Circuits and Systems, MIXDES'2004, Szczecin, pp. 199-203.

[Sniatala03]
Savakis A., **Śniatała P.**, Rudnicki R., "Real Time Video Annotation Using MPEG-7 Motion Activity Descriptors", Proc. of 'Mixed Design of Integrated Circuits and Systems', MIXDES'2003, Lodz, Poland, June 2003, pp 625-628.

6. **Industrial cooperation**

- Participation in NCBIR grant "Intelligent system for pavement condition monitoring" – author is responsible for computer tools implementation, which can be used to extract a pavement crack detection, based on given images data base.;
- Participation in designing and implmenetation of SCADA system in the water treatment station "Zakład Północny w Wieliszewie", Miejskie Przedsiębiorstwo Wodociągów i Kanalizacji w m.st. Warszawie S.A.
- supervision of the implementation of the telecom engineering system in Wrocław airport.
- Participation in preparation of several expertizes of SCADA systems and BMS (ang. Building Management System) for gas and power electric industry

7. **Teaching activity**

Author was presented many courses both in Poland and abroad. Some example courses are listed below:

Polish universities:

- Electronics
- VLSI design
- Hardware signal processing
- Hardware image processing
- Introduction to Computer Science
- CAE for digital and analog circuits design
- Hardware description languages for digital circuits – VHDL
- Digital circuits design
- Circuits and Systems
- Numerical Methods
- C++ programming

Rochester Institute of Technology, USA – 4 years, Nova University Lisbon – 3 x 1 month):

- VLSI Design
- Advanced VLSI Design
- Introduction to Digital Systems
- Digital Systems Design
- Hardware Description Languages
- Assembly Language Programming
- Mixed Systems Design

2013 – Poznan University of Technology Rector's award for teaching.

8. **International experiences**

- 1998 – 2002 (4 years)
  Visiting Assistant Professor (od 2000r. etat "tenure track" - Assistant Professor)
  Rochester Institute of Technology, Department of Computer Enginering,
  Rochester, NY USA.

- 2014 (1 month)
  Lectures, research activity
  Rochester Institute of Technology, Department of Computer Enginering, Department of Computer Science.
  Rochester, NY USA.

- 2013 (1 month)
  Universidade Nova de Lisboa – Faculty of Science and Technology
  Lectures, research activity.

- 2010 (1 week)
  Universidade Nova de Lisboa – Faculty of Science and Technology
  Consulting in project IMPACT, participation in Ph.D. committee.

- 2007 (1 week)
  Universidade Nova de Lisboa – Faculty of Science and Technology
  Lectures - ERASMUS teaching staff activity.

- 1998 (1 week)
  MicroEngineering, Course: IC Processing Engineering,
  Rochester Institute of Technology,
  Rochester, NY USA.

- 1997 (1 week)
  Hogeschool Enschede, Holandia, Course: Analog design in Compass

- (1 week)
  ETH Zentrum, Zurich, Szwajcaria.

9. **Organizing activity**
   - Research and teaching cooperation with Nova Univeristy, Lisbon. Participation in Master and Ph.D. committees.
   - Cooperation in Erasmus-Socrates program with University Nova Lisbon (Portugal) and Linkoping University (Sweden).
   - Coordinator of Erasmus-Socrates program at the department level at PUT.
   - Organization and maintenance of reprogrammable lab - I was granted a project (from industry) to buy the required equipment for the lab.
   - Students' internship coordinator
   - Participation in European projects:
     - „Z transferem na TY – staże i szkolenia praktyczne dla pracowników naukowych i naukowo-dydaktycznych uczelni" (2012)
     - "Knowledge engineering for smart growth", Project "Kapitał Ludzki" (2014)

10. **Grants**
    - "Low Power Design for Mixed Analog-digital Integrated Circuits", Grant MNiSW, (contractor).
    - "Design and Simulation of Macro Cell for Mixed Signal Systems in FPGA Environment", Grant KBN - Poland, (contractor).
    - "Hardware Implementation of Document Image Processing Algorithm", USA, Rochester Institute of Technology (RIT), (contractor).

- “Web Based VHDL library for Multimedia Processing Algorithms”, USA, RIT (Prime contractor).
- “Low Power Design for Mixed Analog-digital Integrated Circuits”, USA, RIT (Prime contractor).
- „Design and prototype implementation of control and telemetry systema for gas burners” – Grant MNiSW, (contractor).
- Expertize for PGNiG (Prime contractor)