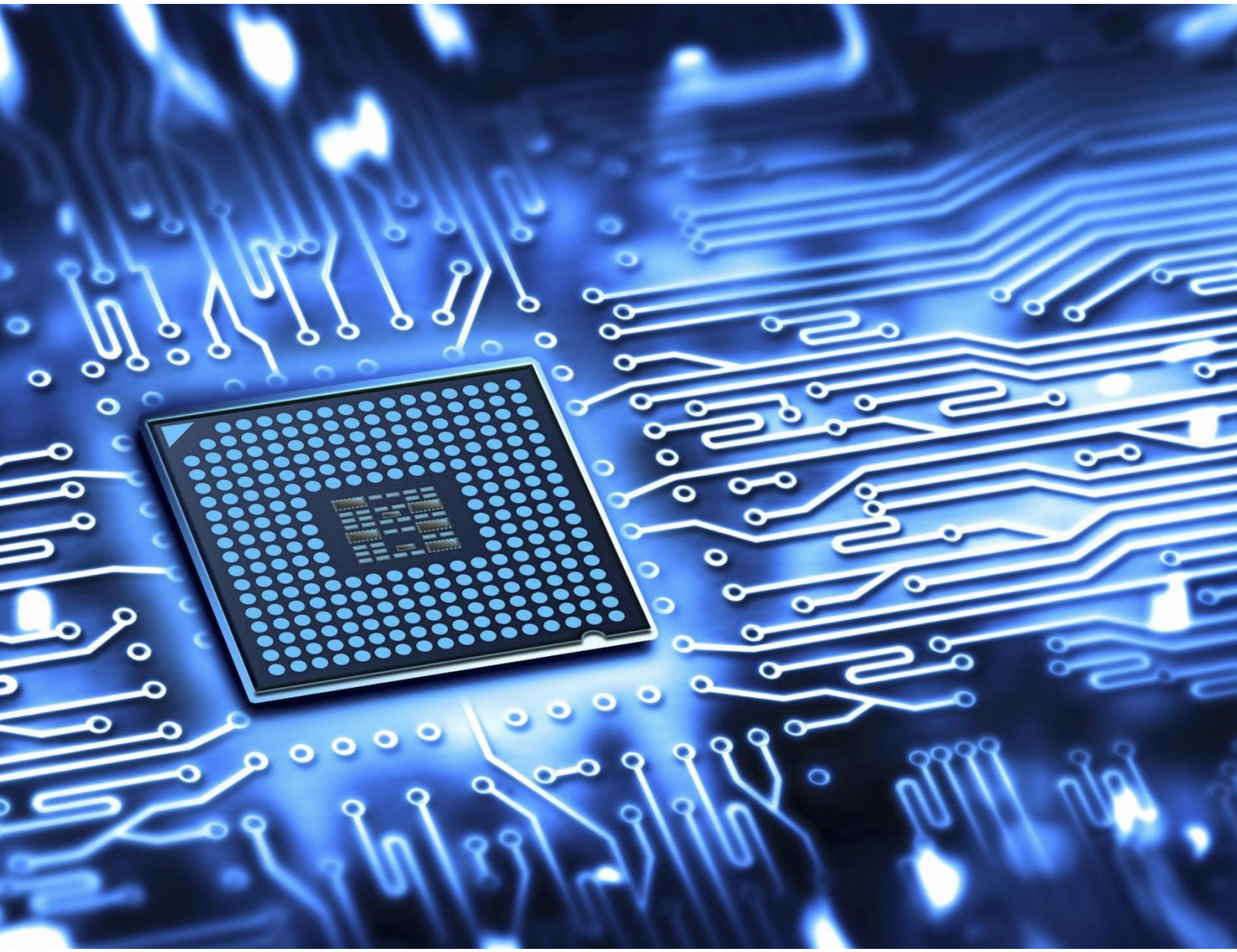
Integrated & Embedded Systems Laboratory



Current-Mode Field Programmable Analog Array

Poznan 2016

Current-Mode FPAA

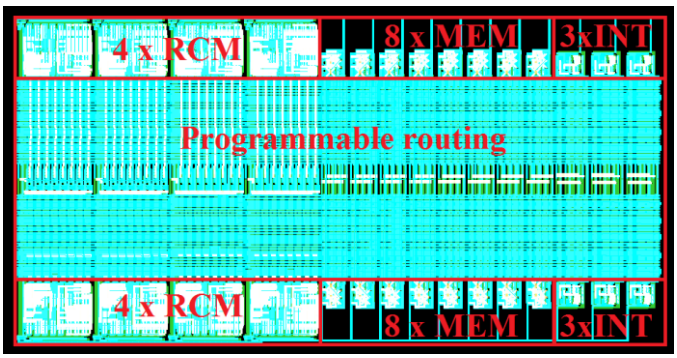
Field Programmable Analog Array

Abstract

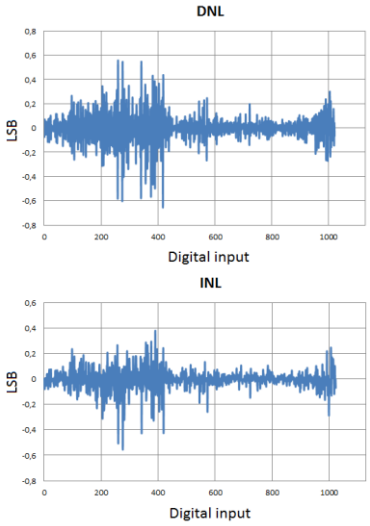
Under the Departmental Research Projects for Supporting the Development of Young Scientists (DSMK), the chair raised funds to subsidize research on a reprogrammable analog matrix and a fully digital matrix interface. The goal of the research was to develop an FPAA type architecture and an environment for synthesizing circuits using the developed architecture.

Highlights / Key features

FPAA which can be implemented in modern nanometre CMOS technologies; tools for synthesizing analogue circuits identical with solutions for digital circuits; assigning features of synthesizability to the VHDL-AMS language; tools for designing sigma-delta modulators; decoupling designing analog circuits from the dispersion phenomena; using SI circuits in amperometry; perceptron with competitive parameters; reconfigurable DAC converter;

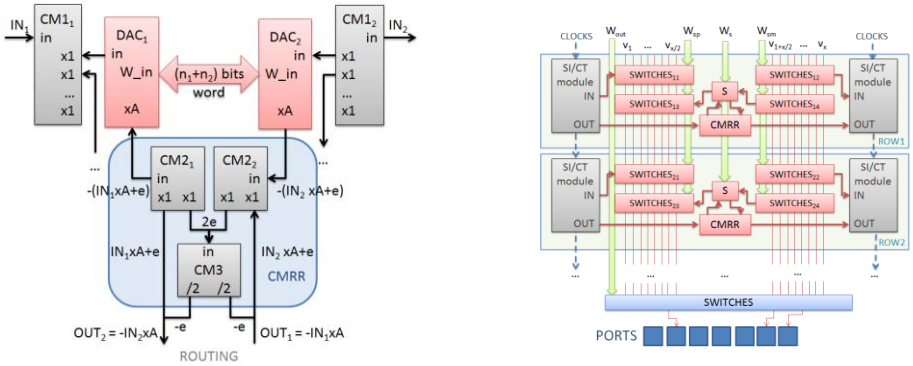


Layout of FPAA IPcore



High precision hardware signal processing

The research was funded under the two following projects:
2014 – Synthesis of mixed circuits on a reconfigurable SI matrix
2015 – SI reconfigurable matrix interface



Programmable modules and routing

The scope of the research included implementation of a programmable architecture working in the current mode, developing tools for synthesizing, corresponding to digital implementations, performing a sample synthesis of circuits (filters, image processors, neural networks), an analysis of operation of circuits in the weak inversion mode, an analysis of immunity to mismatch and designing ADC and DAC converters based on sigma-delta modulators.

Synthesis Tools for Current-Mode FPAA

Abstract

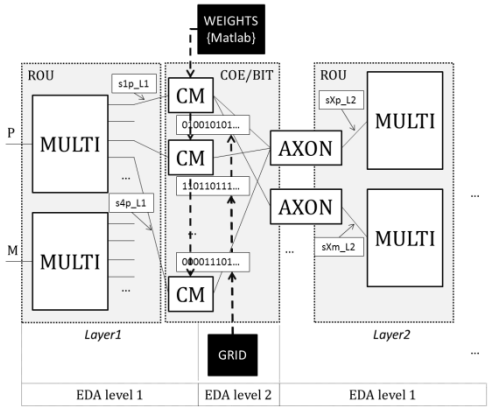
The study demonstrates original tools for synthesizing and implementing current-mode analog circuits in the Field Programmable Analog Array (FPAA) technology. The tools are compatible with the existing hardware architecture description standards (VHDL-AMS, HSPICE) and the existing EDA software. The tools are also equipped with the option of debugging a programmed circuit.

Highlights / Key features

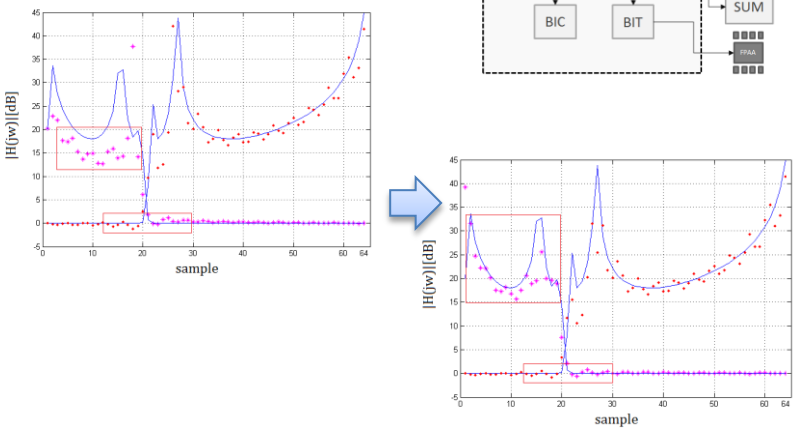
analog current-mode circuits synthesis; automating the design process; debugging analog devices

CAD Tool

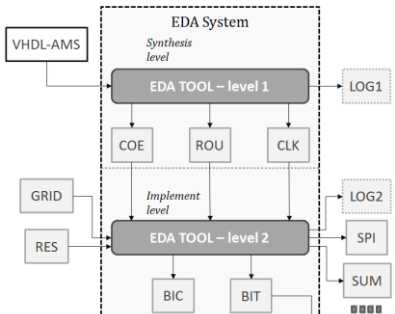
- Implementing synthesis tools dual to existing digital solutions
- Making the design process independent on the architecture
- Assigning features of synthesizability to the VHDL-AMS language
- Using common hardware description standards
- Developing a method for debugging analog devices
- Compatibility with the existing tools



Synthesis of a neural network working in the current mode



Analog devices debugger



Main Contributions

S. Szczęsny, Current-Mode FPAA with CMRR Elimination and Low Sensitivity to Mismatch, Accepted for publishing in Circuits, Systems & Signal Processing, 2016, IF=1.178

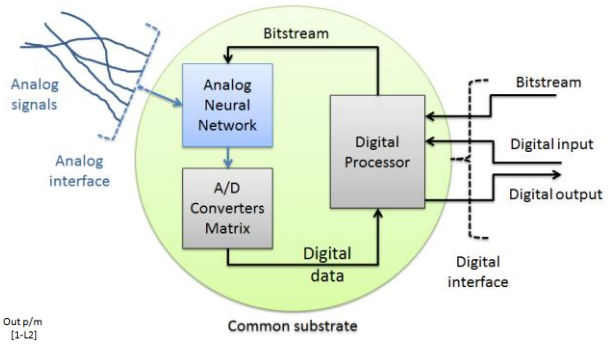
S. Szczęsny, High Speed and Low Sensitive Current-Mode CMOS Perceptron, Microelectronic Engineering, vol. 165, pp. 41-51, 2016, IF=1.197.

Current-Mode FPAA

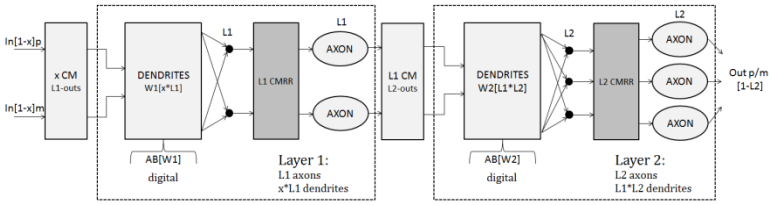
Analog CMOS perceptron

Implementation of a CMOS high speed and low sensitive current mode CMOS perceptron:

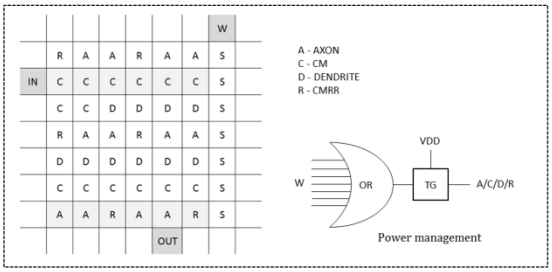
- axon with a monotonic, differentiable and sigmoid activation function
- reducing power consumption and CMRR component elimination
- transistor axon and programmable dendrite prototypes
- elimination of the mismatch process
- analog network implemented in a digital technology
- 85k transistors, 1098 multipliers
- precision = 94.62%, high FoMs



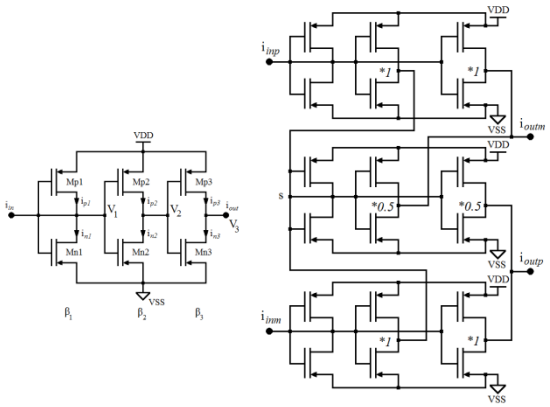
Mixed computional neuroscience system



Routing of a perceptron working in a balanced structure



Floorplan of a network ready for implementing in a row topography



Axon a) and dendrite b) transistor prototypes

Main Contributions

S. Szczęsny, Current-Mode FPAA with CMRR Elimination and Low Sensitivity to Mismatch, Accepted for publishing in Circuits, Systems & Signal Processing, 2016, IF=1.178

S. Szczęsny, High Speed and Low Sensitive Current-Mode CMOS Perceptron, Microelectronic Engineering, vol. 165, pp. 41-51, 2016, IF=1.197

S. Szczęsny, M. Kropidłowski, M. Naumowicz, P. Śniatała, EDA tools for designing ∑Δ modulators working in the current-mode, Przeglad Elektrotechniczny, vol. 92, Issue 9, pp. 77-80, 2016

S. Szczęsny, M. Naumowicz, A. Handkiewicz, M. Melosik, FPAA Accelerator for Machine Vision systems, KKE 2015 (Distinction of the KKE Scientific Committee)