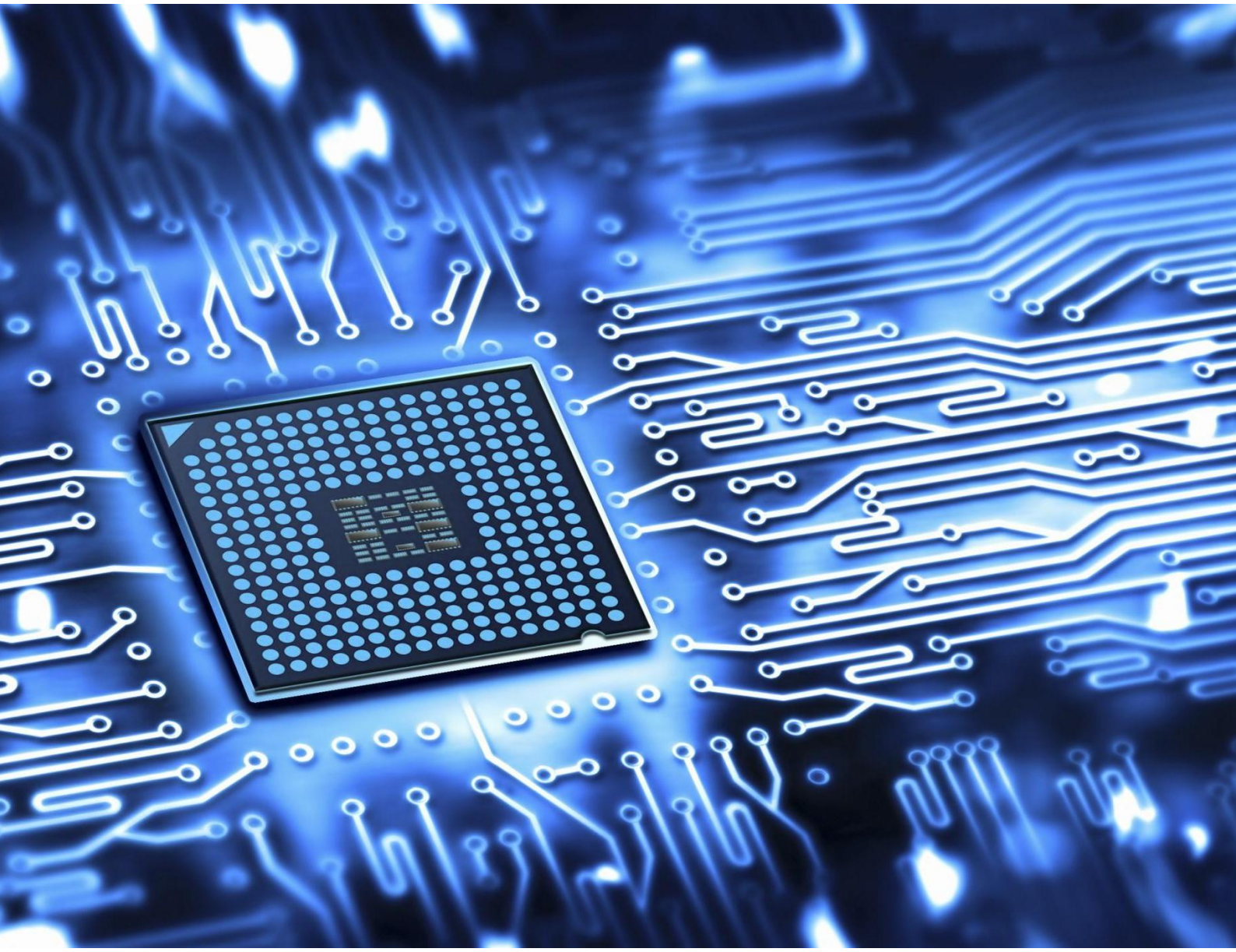
Integrated & Embedded Systems Laboratory



CMOS Mixed-Signal Processing

Poznan 2016

Discrete Cosine Transform (DCT) implemented in SI technique

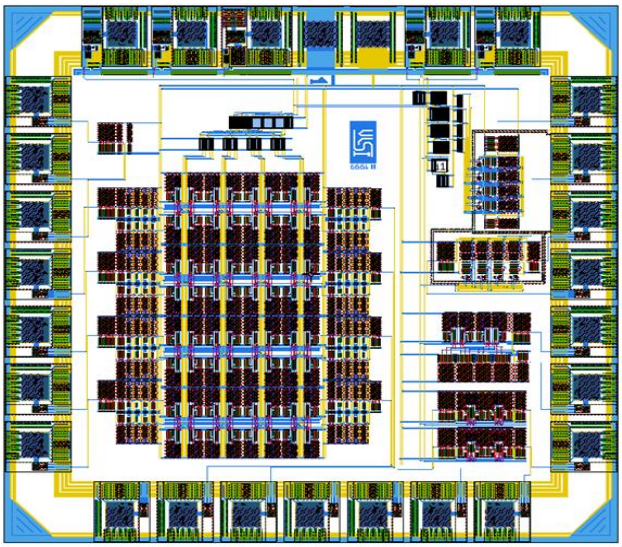
Abstract

The discrete cosine transform (DCT) helps separate the image into parts (or spectral sub-bands) of differing importance (with respect to the image's visual quality). The DCT is similar to the discrete Fourier transform: it transforms a signal or image from the spatial domain to the frequency domains. DCT is a basis of the JPEG compression standard. The basic purpose of these operations is to take a signal and transform it from one type of representation to another. For example, an image is a two-dimensional signal that is perceived by the human visual system. The DCT can be used to convert the signal (spatial information) into numeric data ("frequency" or "spectral" information) so that the image's information exists in a quantitative form that can be manipulated for compression.

Highlights / Key features

The prototype chip was designed with the help of Compass Automation Tools and fabricated in Austria Microsystems AMS CYE 0.8 µm. The presented chip implements the DCT transform in a circuit realized in the SI technique. The prototype chip includes also modified version of the SI integrators. Size: 961.8µm x 1064.0µm

Chip Design and Implementation



The Discrete Cosine Transform implemented in SI technique

Main Contributions

Handkiewicz, A., Śniatała, P., Pałaszyński, G., Szczęsny, Sz., Katarzyński, P., Melosik, M., Naumowicz, M., "Automated DCT Layout generation using AMPLE language" Zeszyty Naukowe nr 256 Uniwersytet Technologiczno-Przyrodniczego w Bydgoszczy, Telekomunikacja i Elektronika 13 (2010), pp.5-14.

Handkiewicz, A., Śniatała, P. ,Pałaszyński G., Szczęsny S., Katarzyński P., Melosik M., Naumowicz M., "Automated DCT layout generation using AMPLE language", Proceedings of the 17th International Conference Mixed Design of Integrated Circuits and Systems, MIXDES' 2010, pp. 215 – 218, ISBN 978-1-4244-7011-2.

Szczęsny Sz., Kropidłowski M., Handkiewicz A., Melosik M., Śniatała P. "2D DCT compression in the switched-current technique", Przegląd Elektrotechniczny, R. 90 NR 9/2014, pp.94-97, ISSN 0033-2097.

Nonlinear digital filter for video restoration

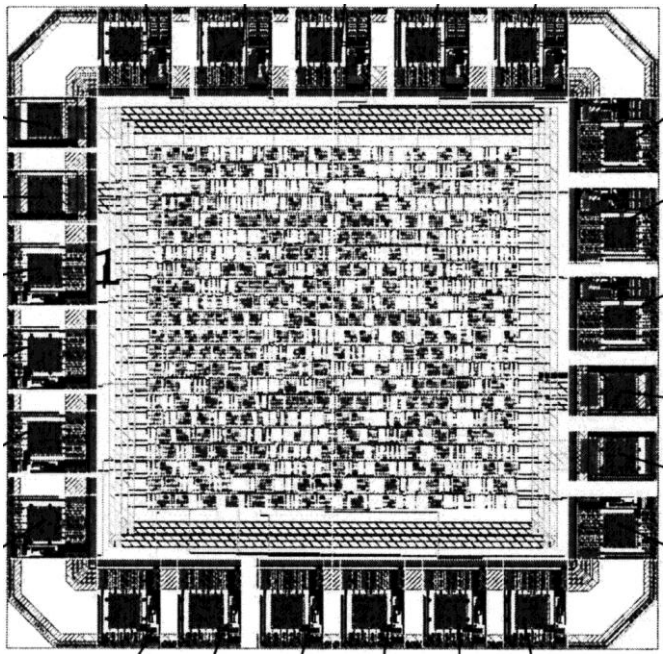
Abstract

Impulsive noise is a model of quite many types of image and video degradation produced both during acquisition and transmission. Therefore rejection of impulsive noise is one of important tasks of image restoration. Many types of nonlinear filters have been already proposed and examined for this task. Among them median filters and their variants should be considered as the most popular filter types used for impulsive noise rejection. Their fundamental advantage is edge preservation. The chip contains of a nonlinear digital filter for video restoration implemented as an ASIC in AMS 0.6 μm CMOS technology.

Highlights / Key features

The prototype chip was designed with the help of Cadence Tools and fabricated in Austria Microsystems AMS 0.6 μm CUP 5.5V with 3 metal layers (via CMP). Size: 1884μm x 1884μm.

Chip Design and Implementation



The digital nonlinear filter for video restoration

Main Contributions

Domański, M., Handkiewicz, A., Kropidłowski, M., Łukowiak, M., "0.6 um CMOS implementation of a nonlinear filter for video restoration", International Conference on Signals and Electronic Systems, Łódź, Poland, 18-21 September 2001, pp. 229-234,

SI filter pair and filter bank

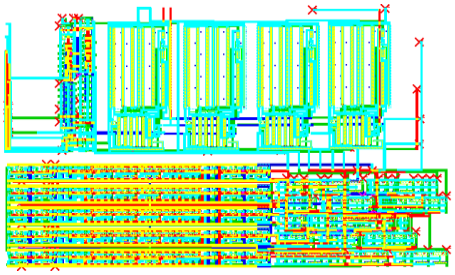
Abstract

A pair of 5th order filters and a filter bank containing three pairs of 5th order filters designed and manufactured in the 180 nm CMOS technology. These circuits are, most probably, the most complex circuits ever developed in the switched currents technique. The circuits were designed under a grant Automation of analogue integrated circuits implemented in the switched currents technique (no. N N515 242937, NCN). Results of measurements of real circuits were published in JCR journals.

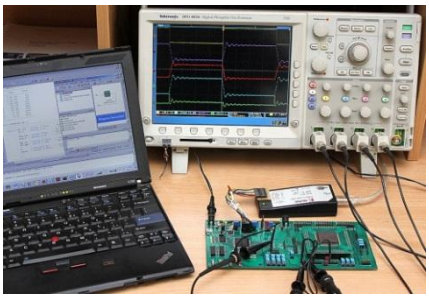
Highlights / Key features

the first fully automatically designed SI layout – an example of using the SI-Studio environment; filter bank with an SI circuit of the highest complexity in history; using digital techniques for designing analogue circuits; topography optimized for power consumption, work speed and area occupancy;

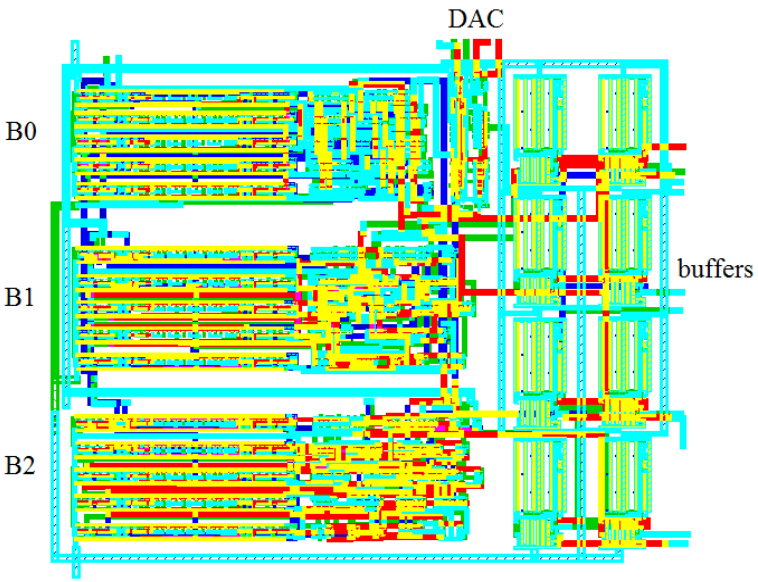
Chip Design and Implementation



5th order filter pair topography



Chip measurement setup



Filter bank topography

Main Contributions

A. Handkiewicz, S. Szczęsny, M. Naumowicz, P. Katarzyński, M. Melosik, P. Śniatała, M. Kropidłowski, SI-Studio, a layout generator of current mode circuits, Expert Systems with Applications, vol. 42, Issue 6, pp. 3205-3218, 2015, IF = 2.24

Szczęsny Sz.; Naumowicz M.; Handkiewicz A., SI-Studio – environment for SI circuits design automation, Bulletin of the Polish Academy of Sciences, Technical Sciences, vol. 60, Issue 4, p. 757-762, 2012, IF = 0.914

A. Handkiewicz, S. Szczęsny, M. Naumowicz, M. Melosik, P. Katarzyński, Generation of SI filters layout using the row strategy, Przegląd Elektrotechniczny, vol. 87, Issue 10, pp. 80-83, 2011