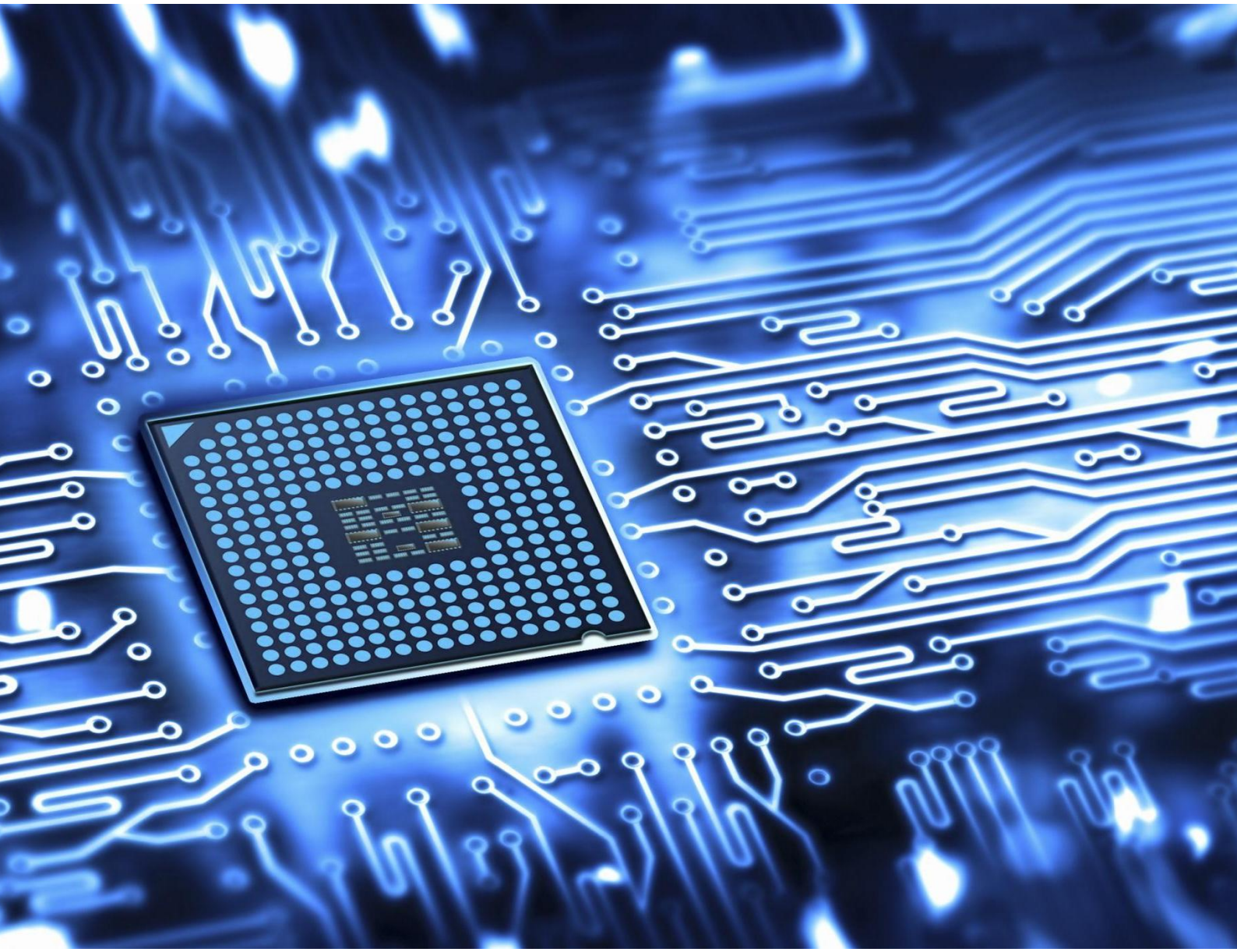
Integrated & Embedded Systems Laboratory



CMOS Current Mode Sigma-Delta Modulators

Poznan 2016

3rd order elliptic filter and Sigma-Delta modulator implemented in SI technique

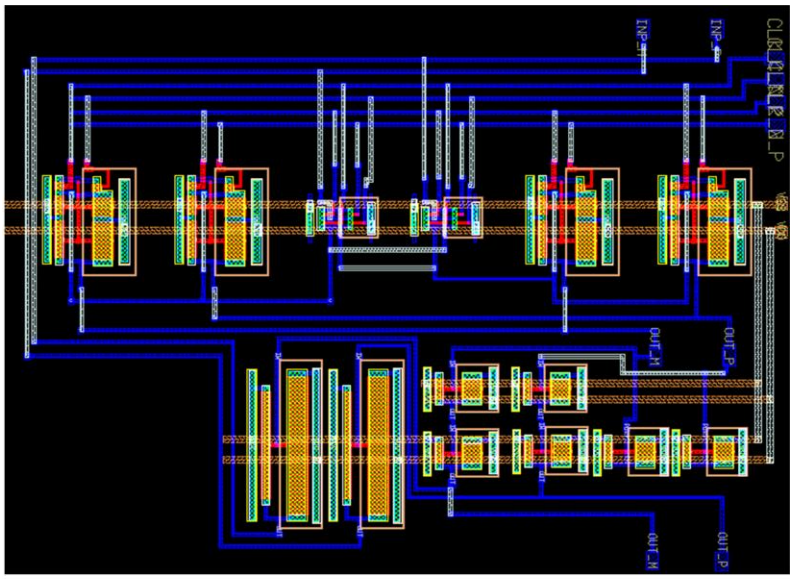
Abstract

The ability to implement analog circuitry in standard digital CMOS processes allows the cheap fabrication of complete mixed-signal systems on a chip. Two key components of mixed-signal systems are the Analog to Digital Converter (ADC) and the Digital to Analog Converter (DAC), both of which can be implemented using Sigma-Delta Modulators. More complex circuitry is also possible as any discrete time linear system can be implemented using SI since these systems can be constructed from three elements: a summer, a multiplier/scaling element and a delay element. All three of these can be implemented in SI: through nodes at which two or more currents add, current mirrors and SI memory cells, respectively.

Highlights / Key features

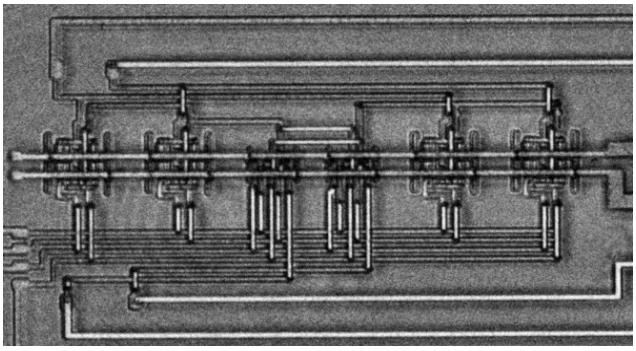
The first prototype chip was prepared in AMS 0.35 _m CMOS C35B4C3 technology and produced through CMP. This technology offered 4-metal, double-poly, 3.3 V power supply. The design was created with the help of Mentor Graphic Tools and fabricated in Austria Microsystems AMS 0.35µm CMOS C35. Size: 2200 µm x 2050 µm

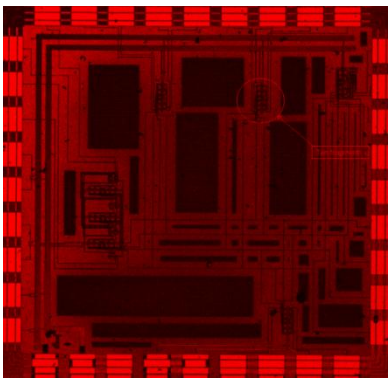
Chip Design and Implementation



a) filter layout **b) chip's package**

CMOS Current Mode Sigma-Delta





micro-photos of the chip

Main Contributions

Handkiewicz A., Katarzyński P., Szczęsny S., Wencel J., Śniatała P. ; “Analog filter pair design on the basis of a gyrator–capacitor prototype circuit”, International Journal of Circuit Theory and Applications, 2012, vol.40, no.6, pp.539-550. IF=1.759, F=32

Handkiewicz A., Katarzyński P., Szczęsny S., Naumowicz M, Melosik M., Śniatała P., “VHDL-AMS in SI (switched-current) analog filter pair design based on a gyrator-capacitor prototype circuit”, International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, DOI: 10.1002/jnm.1921, Vol.27, pp.268-281, March 2014.
F-15, IF=0.615

CMOS Current Mode Sigma-Delta

Modified version of Sigma-Delta modulator implemented in SI technique

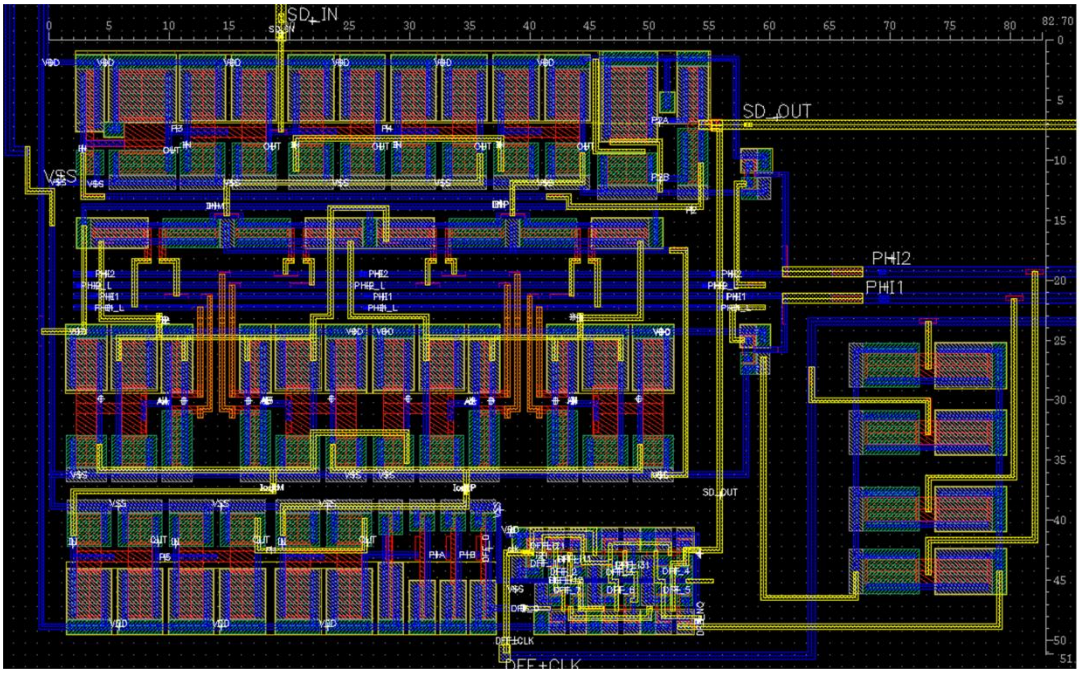
Abstract

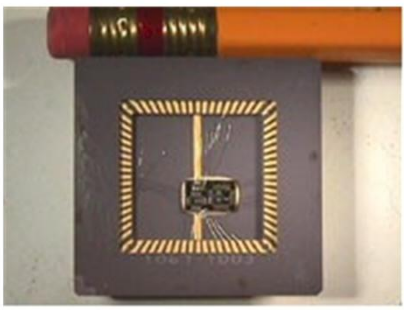
The next two implementations of the testing structures were fabricated in the TSMC 0.18 μm, single poly, six metal, salicide CMOS process. The recommended nominal supply voltages are 3.3 V and 1.8 V. The designed chips were prepared for low voltage (1.8 V). The second version of the SI modulator features an integrator with the CMMR compensation block and the comparator with the Schmitt block and direct current outputs.

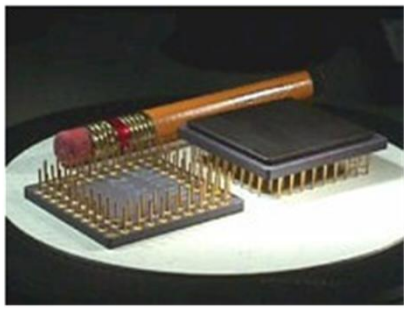
Highlights / Key features

The prototype chip was designed with the help of Mentor Graphic Tools and fabricated in Austria Microsystems AMS AMS 0.35μm CMOS C35. Size: 2200 μm x 2050 μm

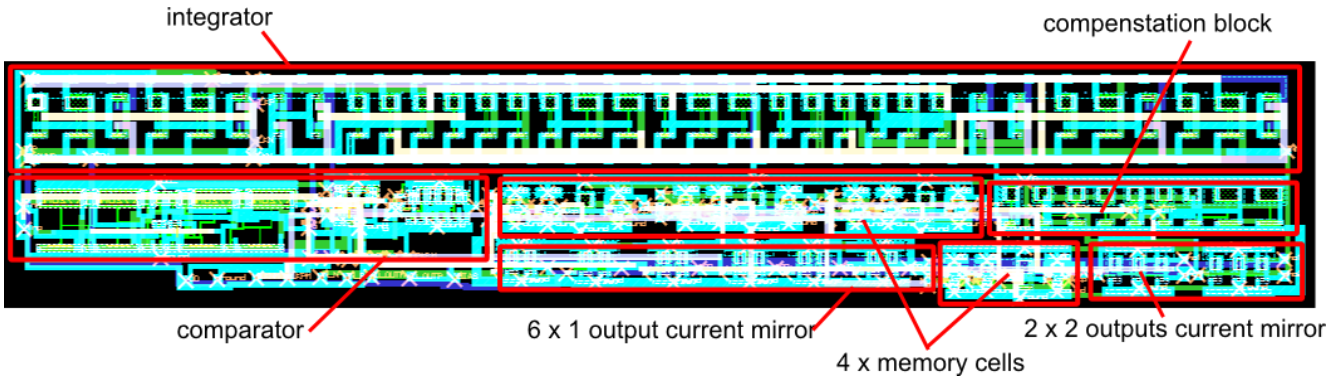
Chip Design and Implementation







Layout and the chip of the first version of the Sigma-Delta modulator implemented in TSMC 0.18 μm.



Layout of the second version of the Sigma-Delta modulator in TSMC 0.18 μm

Main Contributions

Śniatała P., Botha A.S., „A/D converter based on a new memory cell implemented using the switched current technique", Microelectronics Reliability vol.44, 2004, pp.861-867. IF=0.607, F=8

Śniatała P., Handkiewicz A., Szczęsny S., Naumowicz M., Melo J., Paulino N., Goes J., "Current mode sigma-delta modulator designed with the help of transistor's size optimization tool", Bulletin of the Polish Academy of Sciences, Technical Sciences, Vol. 63, No. 4, 2015. DOI: 10.1515/bpasts-2015-0104 . IF=0.914, F=25

Handkiewicz A., Katarzyński P., Szczęsny S., Naumowicz M., Melosik M., Śniatała P., Kropidłowski M., "Design automation of a lossless multiport network and its application to image filtering", Expert Systems With Applications, pp.2211-2221, vol 41, Issue 5, 2014 ISSN 0957-4175. IF=2.24, F=35,

Handkiewicz A., Szczęsny S., Naumowicz M., Katarzyński P., Melosik M., Śniatała P., Kropidłowski M., "SI-Studio, a layout generator of current mode circuits", Expert Systems With Applications, 2015/4/15, vol.42, no.6 , pp.3205-3218. IF=2.24, F=35

Śniatała P., "VHDL-AMS Descriptions to Accelerate Analog SI Circuits Design", IEEJ International Analog VLSI Workshop, Bordeaux 2005, AVLSIW, No. 47.

Śniatała P., Rudnicki R., "Automated Design and Layout Generation for Switched Current Circuits", Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS 2006), pp. 637-640, ISBN: 0-7803-9390-2.