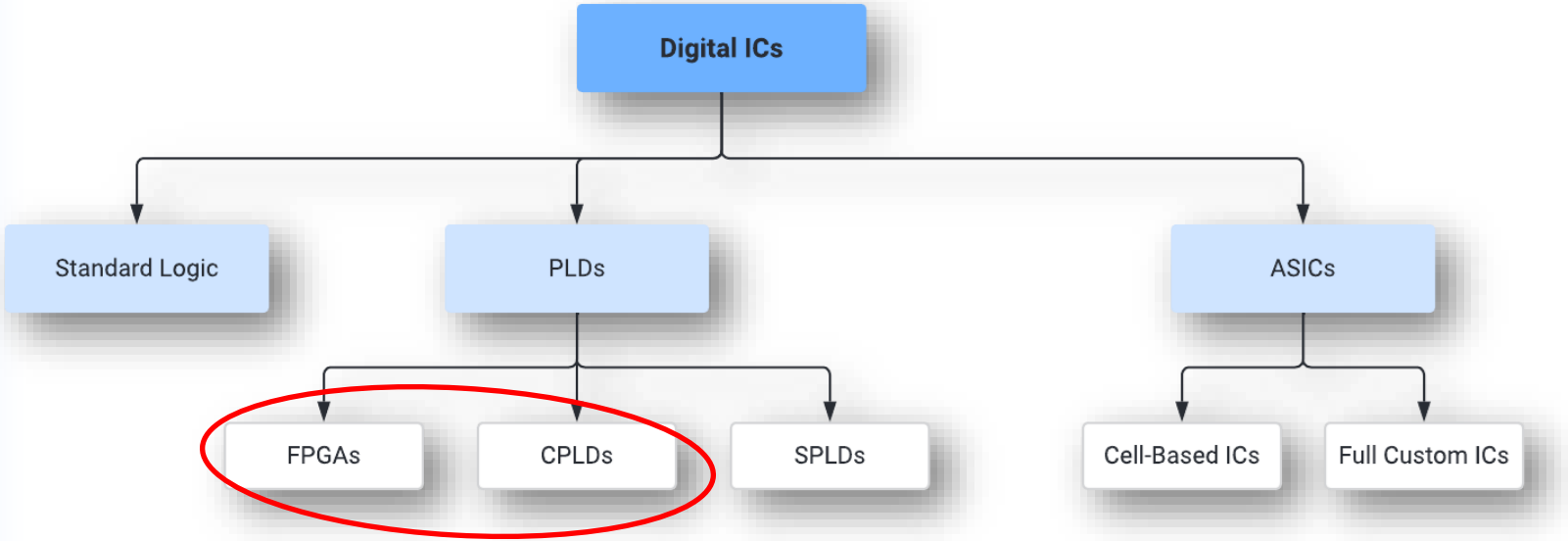
Digital Logic
Design with FPGA

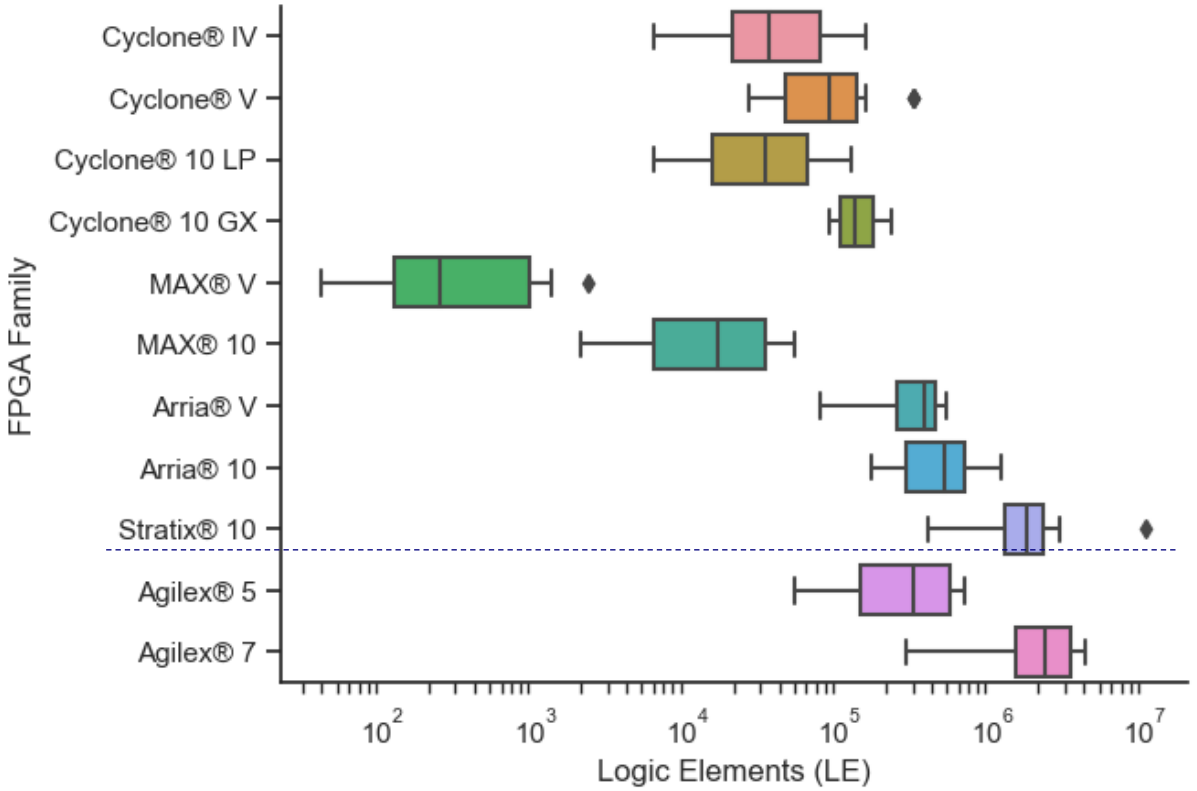
Intel FPGA Architectures

Introduction

Programmable logic devices



Intel® FPGA Families



Digital Logic
Design with FPGA

Intel FPGA Architectures

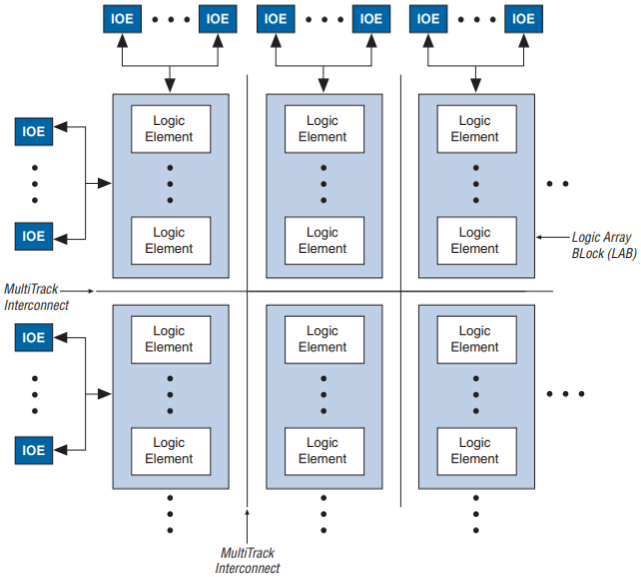
Device and Products (1)

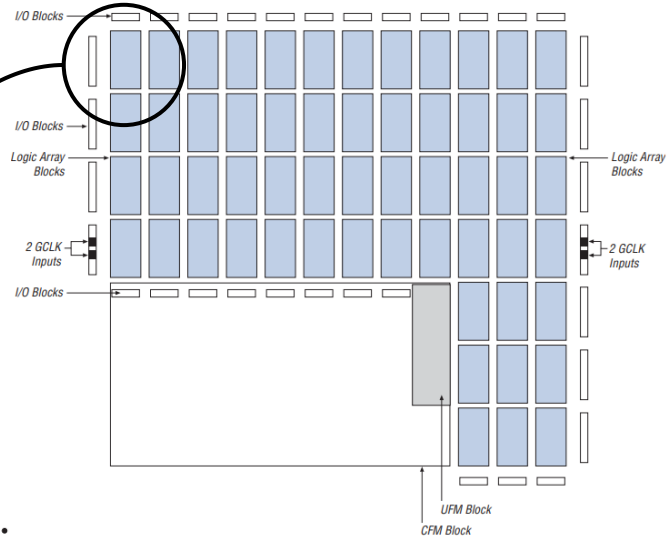
Intel® MAX® V Series

The following list summarizes some of the MAX V device family features:

- Low-cost, low-power, and non-volatile CPLD architecture
- Instant-on (0.5 ms or less) configuration time
- Standby current as low as 25 µA and fast power-down/reset operation
- Fast propagation delay and clock-to-output times
- Internal oscillator

Family was launched in 2010.





Device Floorplan for MAX V Devices

source https://www.intel.com/content/www/us/en/products/details/fpga/max/v/article.html

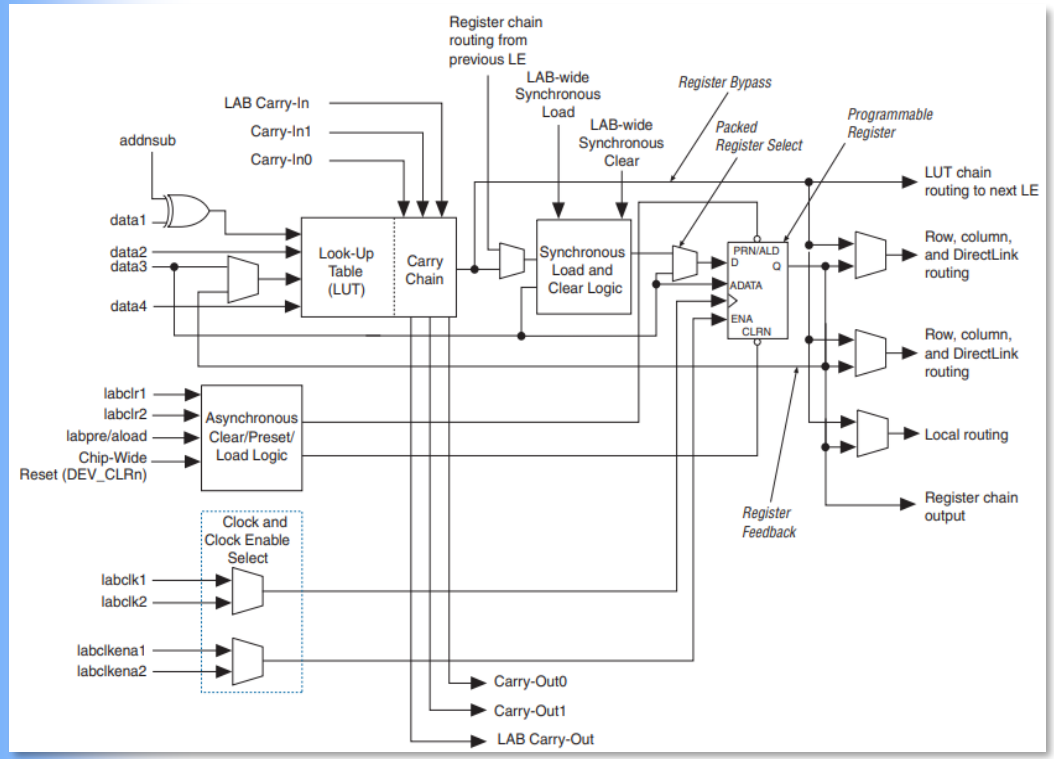
https://www.intel.com/content/www/us/en/content-details/654763/max-v-architecture-max-v-device-handbook-section-i-chapter-2.html

Intel® MAX® V Series

	PRODUCT LINE	MAX V CPLDS[1]						
		5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
Resources	LEs	40	80	160	240	570	1,270	2,210
	Equivalent macrocells[2]	32	64	128	192	440	980	1,700
	Pin-to-pin delay (ns)	7.5	7.5	7.5	7.5	9.0	6.2	7.0
	User flash memory (Kb)	8	8	8	8	8	8	8
	Logic convertible to memory[3]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Clocks, Maximum I/O Pins, and Architectural Features	Internal oscillator	✓	✓	✓	✓	✓	✓	✓
	Fast power-on reset	✓	✓	✓	✓	✓	✓	✓
	Boundary-scan JTAG	✓	✓	✓	✓	✓	✓	✓
	JTAG ISP	✓	✓	✓	✓	✓	✓	✓
	Fast input registers	✓	✓	✓	✓	✓	✓	✓
	Programmable register power-up	✓	✓	✓	✓	✓	✓	✓
	JTAG translator	✓	✓	✓	✓	✓	✓	✓
	Real-time ISP	✓	✓	✓	✓	✓	✓	✓
	MultiVolt I/Os (V)	1.2, 1.5, 1.8, 2.5, 3.3					1.2, 1.5, 1.8, 2.5, 3.3, 5.0[4]	
	I/O power banks	2	2	2	2	2	4	4
	Maximum output enables	54	54	79	114	159	271	271
	LVTTL/LVCMOS	✓	✓	✓	✓	✓	✓	✓
	LVDS outputs	✓	✓	✓	✓	✓	✓	✓
	32 bit, 66 MHz PCI compliant	–	–	–	–	–	✓[4]	✓[4]
	Schmitt triggers	✓	✓	✓	✓	✓	✓	✓
	Programmable slew rate	✓	✓	✓	✓	✓	✓	✓
	Programmable pull-up resistors	✓	✓	✓	✓	✓	✓	✓
	Programmable GND pins	✓	✓	✓	✓	✓	✓	✓
	Open-drain outputs	✓	✓	✓	✓	✓	✓	✓
	Bus hold	✓	✓	✓	✓	✓	✓	✓

source https://www.intel.com/content/www/us/en/content-details/714199/max-v-cpld-features-product-table.html

Intel® MAX® V Logic Elements



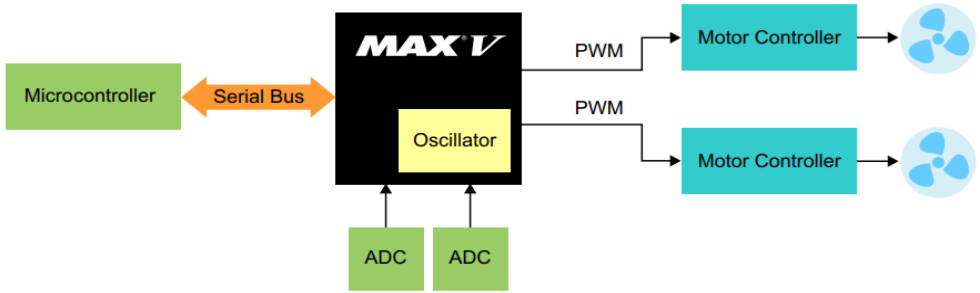
- Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables.
- Each LE contains a programmable register and carry chain with carry-select capability.
- A single LE also supports dynamic single-bit addition or subtraction mode that is selected by an LAB-wide control signal.
- Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and DirectLink interconnects as shown in Figure on the left.

source https://www.intel.com/content/www/us/en/content-details/654763/max-v-architecture-max-v-device-handbook-section-i-chapter-2.html

Intel® MAX® V Applications

With their mix of low price, low power, and high performance, MAX V CPLDs deliver the market's best value. Featuring the industry's first LUT-based, non-volatile architecture and one of the largest CPLD densities, MAX V devices provide higher performance (up to 247.5 MHz) at up to 50 percent lower total power compared to competitive CPLDs. These features allow the following applications to be best served by CPLDs:

- I/O expansion—Performs I/O decoding, which increases the available I/O capability of another standard device with efficiency and at a low cost.
- Interface bridging—Translates bus protocols and voltages between incompatible devices at the lowest possible cost.
- Power management—Manages the power-up sequencing and monitoring of other devices on the board.
- Configuration and initialization—Controls the configuration or initialization of other devices on the board.
- Analog control—Controls analog standard devices (light, sound, or motion) digitally via a pulse-width modulator (PWM), without needing a digital-to-analog converter (DAC).



source https://www.intel.com/content/www/us/en/products/details/fpga/max/v/item.html

Intel® MAX® 10 Series

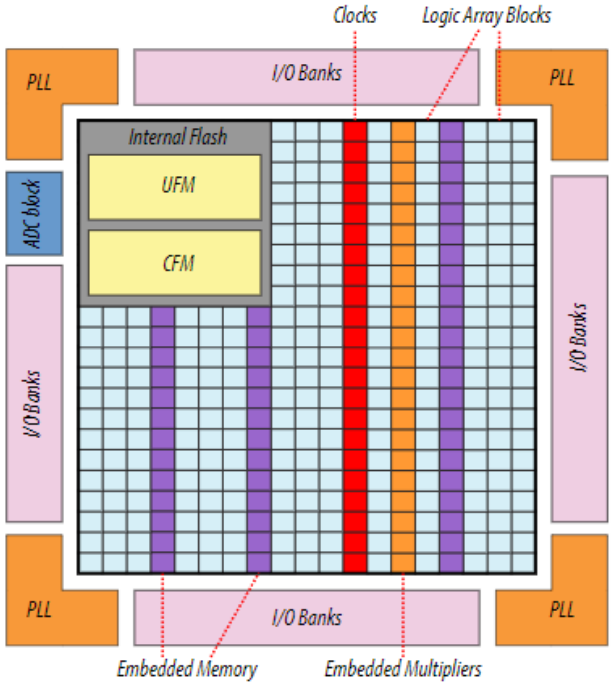
The highlights of the Intel® MAX® 10 devices include:

- Internally stored dual configuration flash
- User flash memory
- Instant on support
- Integrated analog-to-digital converters (ADCs)
- Single-chip Nios II soft core processor support

Family was launched in 2014.

Summary of Intel® MAX® 10 Key Features

- Low cost, small form factor packages—support multiple packaging technologies and pin pitches
- High speed operating frequency and large memory size
- High precision clock synthesis
- Supports up to 600 Mbps external memory interfaces: DDR3, DDR3L, DDR2, LPDDR2 and SRAM



source https://www.intel.com/content/www/us/en/docs/programmable/683658/current/fpga-device-overview.html
https://www.intel.com/content/www/us/en/docs/programmable/683658/current/summary-of-device-features.html

Intel® MAX® 10 Series

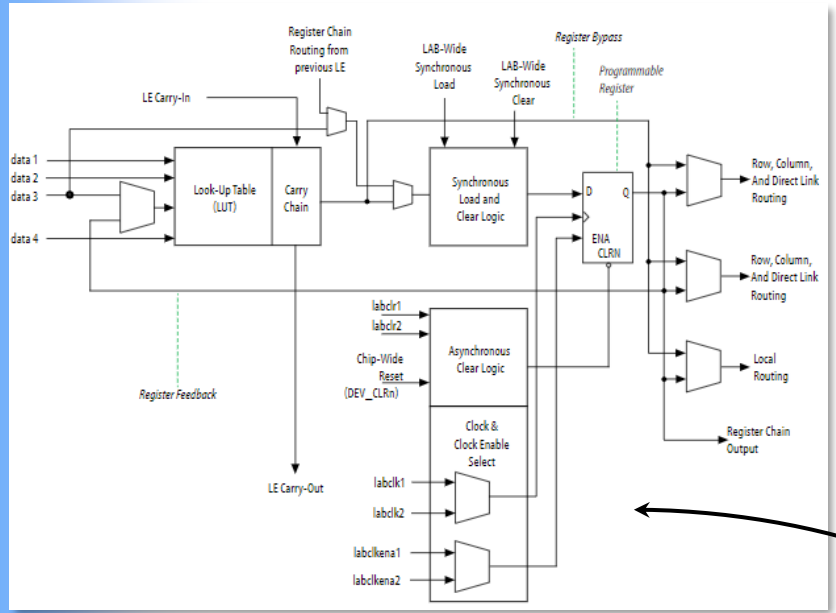
FPGA

Digi

PRODUCT LINE	10M02	10M04	10M08	10M16	10M25	10M40	10M50
LEs (K)	2	4	8	16	25	40	50
Block memory (Kb)	108	189	378	549	675	1,260	1,638
User flash memory[1] (KB)	12	16 – 156	32 – 172	32 – 296	32 – 400	64 – 736	64 – 736
18 x 18 multipliers	16	20	24	45	55	125	144
PLLs[2]	1, 2	1, 2	1, 2	1, 4	1, 4	1, 4	1, 4
Internal configuration	Single	Dual	Dual	Dual	Dual	Dual	Dual
Analog-to-digital converter (ADC), temperature sensing diode (TSD)[3]	-	1, 1	1, 1	1, 1	2, 1	2, 1	2, 1
External memory interface (EMIF)	Yes[4]	Yes[4]	Yes[4]	Yes[5]	Yes[5]	Yes[5]	Yes[5]

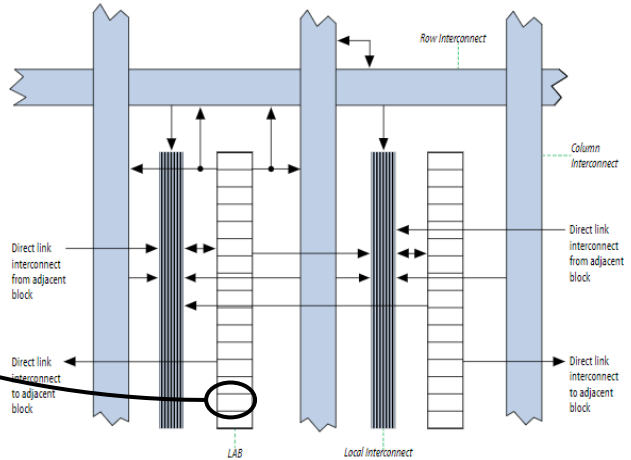
source https://www.intel.com/content/www/us/en/docs/programmable/683658/current/fpga-device-overview.html
https://www.intel.com/content/www/us/en/docs/programmable/683658/current/summary-of-device-features.html

Intel® MAX® 10 Logic Elements



LE High-Level Block Diagram

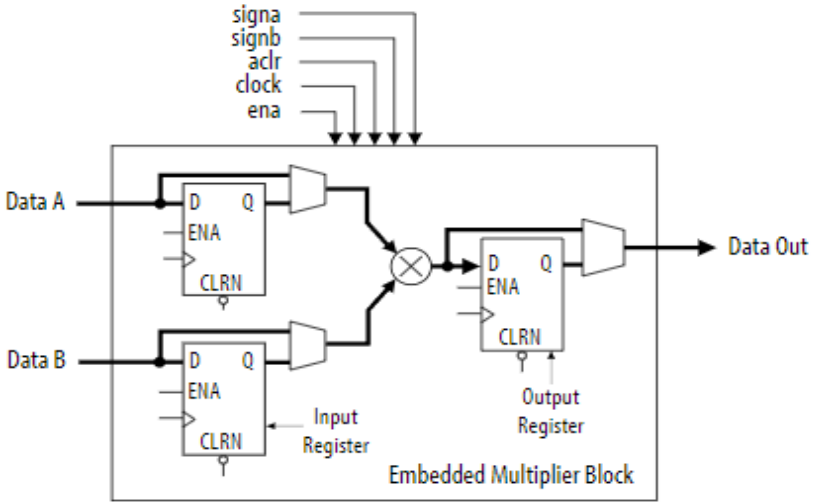
- Each LE input is directed to different destinations to implement the desired logic function.
- Each LE has three general routing outputs.
- Intel® MAX® 10 devices support register packing. With register packing, the LUT or register output drives the three outputs independently.
- Each LE has a register chain output that allows registers in the same LAB (Logic Array Block) to cascade together.
- You can configure the programmable register of each LE for D, T, JK, or SR flipflop operation.
- The register feedback mode allows the register output to feed back into the LUT of the same LE.



source https://www.intel.com/content/www/us/en/docs/programmable/683105/current/le-features.html

Intel® MAX® 10 DSP

- Intel MAX 10 devices support up to 144 embedded multiplier blocks. Each blocksupports one individual 18 × 18-bit multiplier or two individual 9 × 9-bit multipliers.
- Common DSP processing functions such as finite impulse response (FIR), fast Fourier transform (FFT), and numerically controlled oscillator (NCO) functions
- Suites of common video and image processing functions



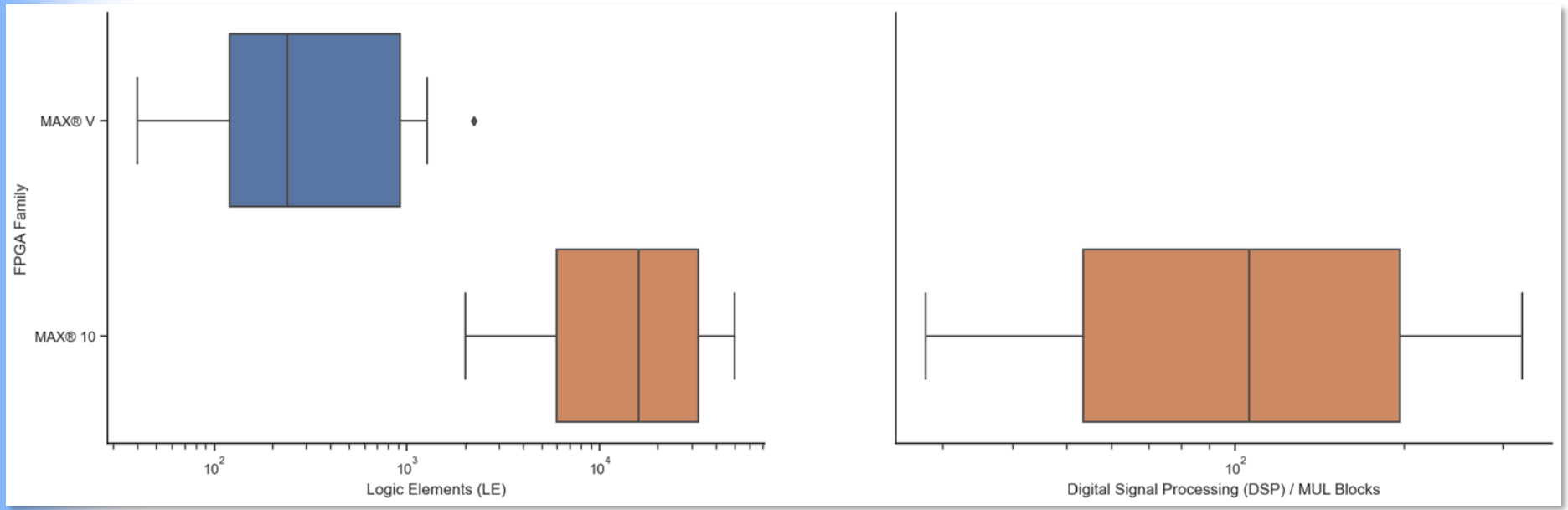
source https://www.intel.com/content/www/us/en/docs/programmable/683658/current/embedded-multipliers-and-digital-signal.html
https://www.intel.com/content/www/us/en/docs/programmable/683467/current/embedded-multipliers-architecture.html

Intel® MAX® 10 Applications

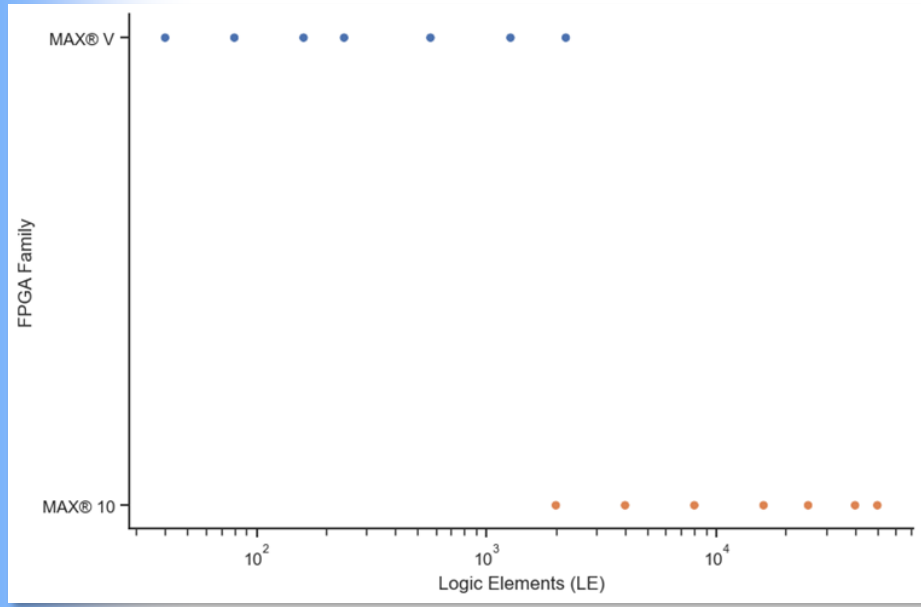
- Suites of common video and image processing functions.
- Board Management Applications - These devices offer power management IC (PMIC) solutions in addition to thermal management support with an integrated on-chip temperature sensing diode.
- Intel® MAX® 10 FPGAs support DDR3 SDRAM and LPDDR2 interfaces through soft intellectual property (IP) memory controllers, optimal for video, datapath, and embedded applications.

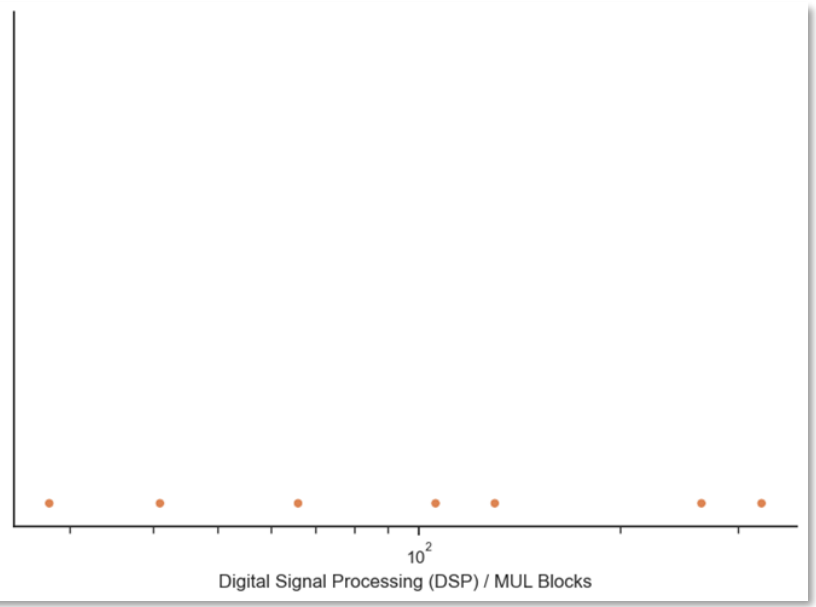
source https://www.intel.com/content/www/us/en/products/details/fpga/max/10.html

Intel® MAX® Differences



Intel® MAX® Differences





Intel® Cyclone®

Cyclone® V FPGAs and SoC FPGAs

- Cyclone® V FPGAs have integrated transceiver variant and SoC FPGA variants with an ARM-based hard processor system (HPS).
- This product family is recommended for Intel Edge-Centric applications and designs.

Cyclone® IV FPGAs

- Cyclone® IV FPGAs are designed for high-volume, cost-sensitive applications to meet increasing bandwidth requirements.

Cyclone® 10 FPGAs

- Intel Cyclone 10 GX FPGAs provide high bandwidth transceivers, LVDS, DDR3 SDRAM, and feature a hard floating-point DSP block.
- Intel Cyclone 10 LP devices offer low static power, cost-optimized functions, and high I/O counts.

source https://www.intel.com/content/www/us/en/products/details/fpga/cyclone.html

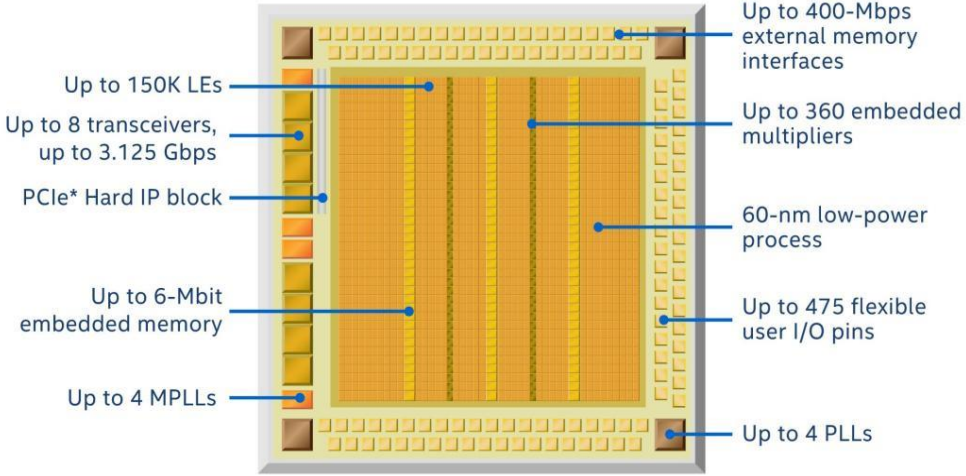
Intel® Cyclone® IV

The Cyclone IV device family offers the following features:

- Low-cost, low-power FPGA fabric:
  - 6K to 150K logic elements
  - Up to 6.3 Mb of embedded memory
  - Up to 360 18 × 18 multipliers for DSP processing intensive applications

- Protocol bridging applications for under 1.5 W total power

The family was launched in 2009.



source https://www.intel.com/content/www/us/en/products/details/fpga/cyclone/iv/article.html

Intel® Cyclone® IV

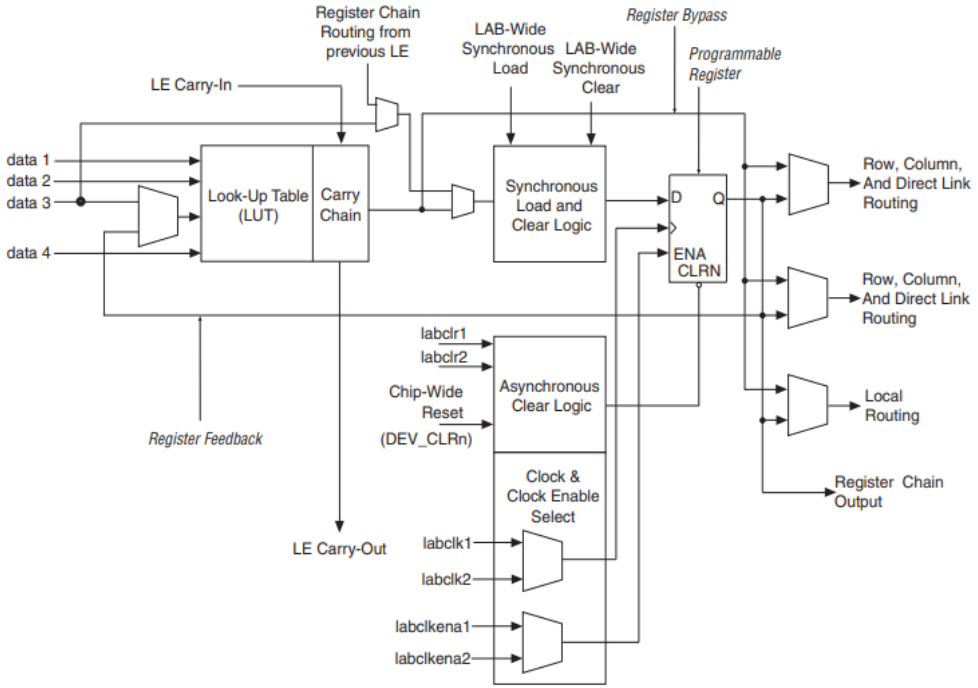
PRODUCT LINE		CYCLONE IV GX FPGAS[1]							CYCLONE IV E FPGAS[1]								
		EP4CGX15	EP4CGX22	EEP4CGX30	EP4CGX50	EP4CGX75	EP4CGX110	EP4CGX150	EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115
Resources	LEs (K)	14	21	29	50	74	109	150	6	10	15	22	29	40	56	75	114
	M9K memory blocks	60	84	120	278	462	666	720	30	46	56	66	66	126	260	305	432
	Embedded memory (Kb)	540	756	1,080	2,502	4,158	5,490	6,480	270	414	504	594	594	1,134	2,340	2,745	3,888
	18 x 18 multipliers	0	40	80	140	198	280	360	15	23	56	66	66	116	154	200	266
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	20	20	20	30	30	30	30	10	10	20	20	20	20	20	20	20
	PLLs	3	4	4	8	8	8	8	2	2	4	4	4	4	4	4	4
	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3															
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12														
	Emulated LVDS channels	9	40	40	73	73	139	139	66	66	137	52	224	224	160	178	230
	LVDS channels, 840 Mbps (receive/transmit)	7/7	14/14	14/14	49/49	49/49	59/59	59/59	–	–	–	–	–	–	–	–	–
	Transceiver count[2] (2.5 Gbps/3.125 Gbps)	2/0	2, 0 / 4, 0	4, 0 / 0, 4[3]	0, 8	0, 8	0, 8	0, 8	–	–	–	–	–	–	–	–	–
	PCIe hardened IP blocks (Gen1)	1	1	1	1	1	1	1	–	–	–	–	–	–	–	–	–
	Memory devices supported	DDR2, DDR, SDR															

Digital

source https://www.intel.com/content/www/us/en/content-details/714186/cyclone-iv-fpgas-family-overview-product-table.html

Intel® Cyclone® IV Logic Elements

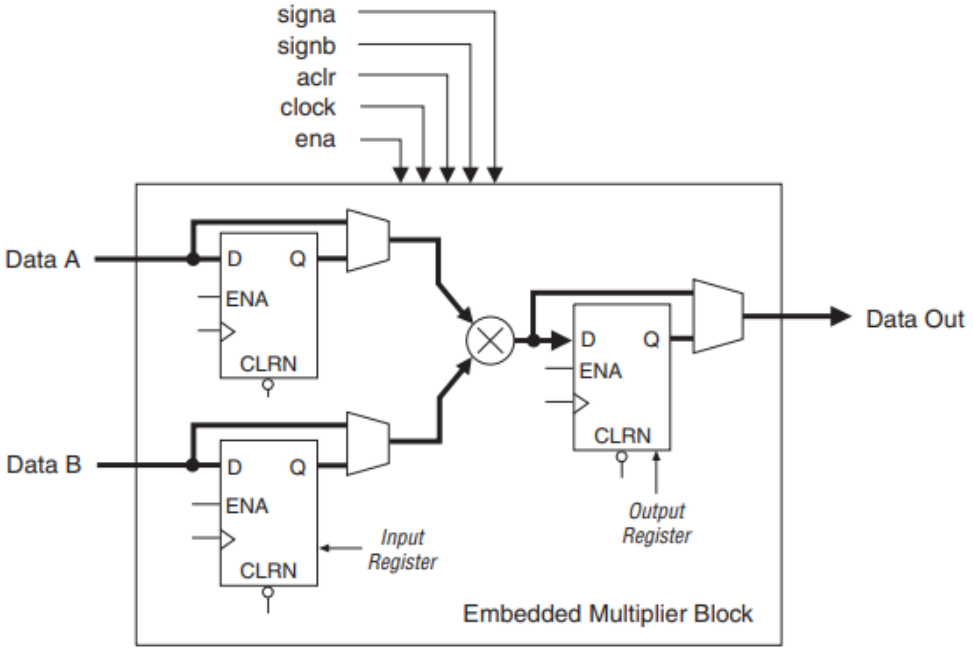
- The fabric consists of LEs, made of 4-input look up tables (LUTs), memory blocks, and multipliers.
- You can configure the programmable register of each LE for D, T, JK, or SR flipflop operation.
- Each register has data, clock, clock enable, and clear inputs.
- Each LE has three outputs that drive the local, row, and column routing resources.



source https://www.intel.com/content/www/us/en/content-details/653677/cyclone-iv-device-handbook-volume-1-chapter-2-logic-elements-and-logic-array-blocks.html

Intel® Cyclone® IV DSP

- The embedded multiplier is configured as either one 18x18 multiplier or two 9x9 multipliers.
- For multiplications greater than 18 × 18, the Quartus® II software cascades multiple embedded multiplier blocks together.
- All input and output registers in a single embedded multiplier are fed by the same clock, clock enable, and asynchronous clear signals.



source https://www.intel.com/content/www/us/en/content-details/654776/cyclone-iv-device-handbook-volume-1-chapter-4-embedded-multipliers.html

Intel® Cyclone® IV Applications

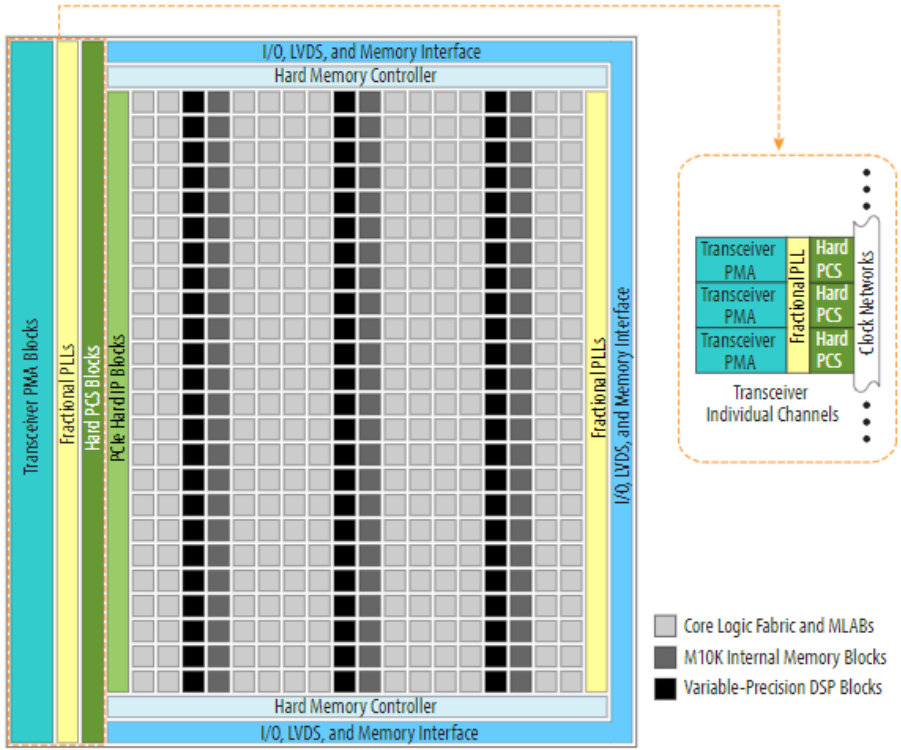
- Cyclone IV FPGAs are well-suited for implementing DSP algorithms. They can be used in applications such as audio processing, image processing, and communications.
- Communications systems for tasks like protocol conversion, data encoding/decoding, and signal processing. They are commonly found in networking equipment, wireless communication systems, and base stations.
- Reducing the power consumption of programmable logic devices carries far-reaching benefits for many applications.

Intel® Cyclone® V

Advantages:

- Lower power consumption
- Improved logic integration and differentiation capabilities
- Increased bandwidth capacity
- Hard processor system (HPS) with integrated Arm® Cortex® -A9 MPCore® processor
- Lowest system cost

This family was launched in 2011.



source https://www.intel.com/content/www/us/en/products/details/fpga/cyclone/v/article.html

https://www.intel.com/content/www/us/en/docs/programmable/683694/current/transceiver-channels.html

Intel® Cyclone® V Family

Cyclone® V E FPGA
- Optimized for lowest system cost and power for a wide spectrum of general logic and DSP applications.

Cyclone® V GX FPGA
- Optimized for lowest cost and power for 614 Mbps to 3.125 Gbps transceiver applications.

Cyclone® V GT FPGA
- FPGA industry's lowest cost and power for 6.144 Gbps transceiver applications.

Cyclone® V SE FPGA
- Integrated ARM® Cortex®-A9 MPCore® Processor System optimized for lowest system cost and power for a wide spectrum of general logic and DSP applications.

Cyclone® V SX FPGA
- Integrated ARM® Cortex®-A9 MPCore® Processor System optimized for lowest cost and power for 614 Mbps to 3.125 Gbps transceiver applications.

Cyclone® V ST FPGA
- Integrated ARM® Cortex®-A9 MPCore® Processor System - FPGA industry's lowest cost and power for 6.144 Gbps transceiver applications.

source https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/item.html

Intel® Cyclone® V

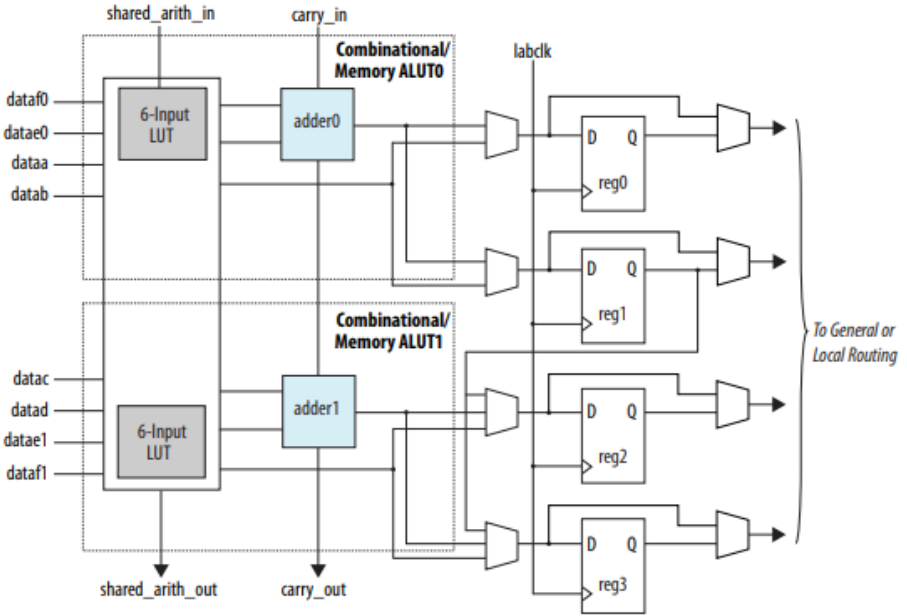
	Product Line	Cyclone V E FPGAs[1]					Cyclone V GX FPGAs[1]					Cyclone V GT FPGAs[1]		
		5CEA2	5CEA4	5CEA5	5CEA7	5CEA9	5CGXC3	5CGXC4	5CGXC5	5CGXC7	5CGXC9	5CGTD5	5CGTD7	5CGTD9
Resources	LEs (K)	25	49	77	149.5	301	35.5	50	77	149.5	301	77	149.5	301
	ALMs	9,434	18,480	29,080	56,480	113,560	13,460	18,868	29,080	56,480	113,560	29,080	56,480	113,560
	Registers	37,736	73,920	116,320	225,920	454,240	53,840	75,472	116,320	225,920	454,240	116,320	225,920	454,240
	M10K memory blocks	176	308	446	686	1,220	135	250	446	686	1,220	446	686	1,220
	M10K memory (Kb)	1,760	3,080	4,460	6,860	12,200	1,350	2,500	4,460	6,860	12,200	4,460	6,860	12,200
	MLAB memory (Kb)	196	303	424	836	1,717	291	295	424	836	1,717	424	836	1,717
	Variable-precision DSP blocks	25	66	150	156	342	57	70	150	156	342	150	156	342
	18 x 18 multipliers	50	132	300	312	684	114	140	300	312	684	300	312	684
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16
	PLLs[2] (FPGA)	4	4	6	7	8	4	6	6	7	8	6	7	8
	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5,3.3												
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12, HiSpi, SLVS, Sub-LVDS												
	LVDS channels (receiver/transmitter)	56/56	56/56	60/60	120/120	120/120	52/52	84/84	84/84	120/120	140/140	84/84	120/120	140/140
	Transceiver count (3.125 Gbps)	–	–	–	–	–	3	6	6	9	12	–	–	–
	Transceiver count (6.144 Gbps)[3]	–	–	–	–	–	–	–	–	–	–	6[4]	9[4]	12[4]
	PCIe hardened IP blocks (Gen1)[5]	–	–	–	–	–	1	2	2	2	2	–	–	–
	PCIe hardened IP blocks (Gen2)	–	–	–	–	–	–	–	–	–	–	2	2	2
	Hard memory controllers[6] (FPGA)	1	1	2	2	2	1	2	2	2	2	2	2	2
	Memory devices supported	DDR3, DDR2, LPDDR2												

	Product Line	Cyclone V SE SoCs[1]				Cyclone V SX SoCs[1]				Cyclone V ST SoCs[1]	
		5CSEA2	5CSEA4	5CSEA5	5CSEA6	5CSXC2	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD6
Resources	LEs (K)	25	40	85	110	25	40	85	110	85	110
	ALMs	9,434	15,094	32,075	41,509	9,434	15,094	32,075	41,509	32,075	41,509
	Registers	37,736	60,376	128,300	166,036	37,736	60,376	128,300	166,036	128,300	166,036
	M10K memory blocks	140	270	397	557	140	270	397	557	397	557
	M10K memory (Kb)	1,400	2,700	3,970	5,570	1,400	2,700	3,970	5,570	3,970	5,570
	MLAB memory (Kb)	138	231	480	621	138	231	480	621	480	621
	Variable-precision DSP blocks	36	84	87	112	36	84	87	112	87	112
	18 x 18 multipliers	72	168	174	224	72	168	174	224	174	224

source https://www.intel.com/content/www/us/en/content-details/714207/cyclone-v-fpga-and-soc-fpfa-family-overview-product-table.html

Intel® Cyclone® V ALM

- One ALM contains four programmable registers. Each register has the following ports:
  - Data
  - Clock
  - Synchronous and asynchronous clear
  - Synchronous load
- Global signals, general-purpose I/O (GPIO) pins, or any internal logic can drive the clock and clear control signals of an ALM register.
- The LUT, adder, or register output can drive the ALM outputs. The LUT or adder can drive one output while the register drives another output.
- The Cyclone V ALM operates in any of the following modes:
  - Normal mode
  - Extended LUT mode
  - Arithmetic mode
  - Shared arithmetic mode



source https://www.intel.com/content/www/us/en/docs/programmable/683375/current/alm-resources.html

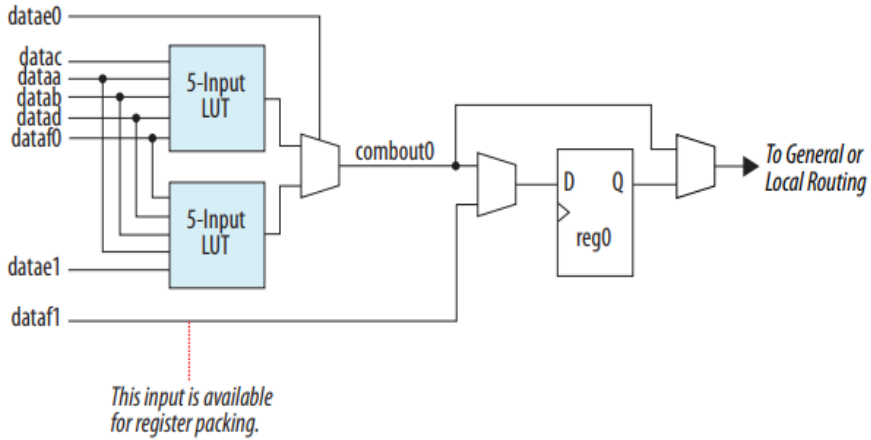
Intel® Cyclone® V ALM Modes

Normal Mode

- Normal mode allows two functions to be implemented in one Arria® V ALM, or a single function of up to six inputs.
- Up to eight data inputs from the LAB local interconnect are inputs to the combinational logic.
- The ALM can support certain combinations of completely independent functions and various combinations of functions that have common inputs.

Extended LUT Mode

- In this mode, if the 7-input function is unregistered, the unused eighth input is available for register packing.
- Functions that fit into the template, as shown in the following figure, often appear in designs as “if-else” statements in Verilog HDL or VHDL code.



source https://www.intel.com/content/www/us/en/docs/programmable/683213/current/extended-lut-mode.html

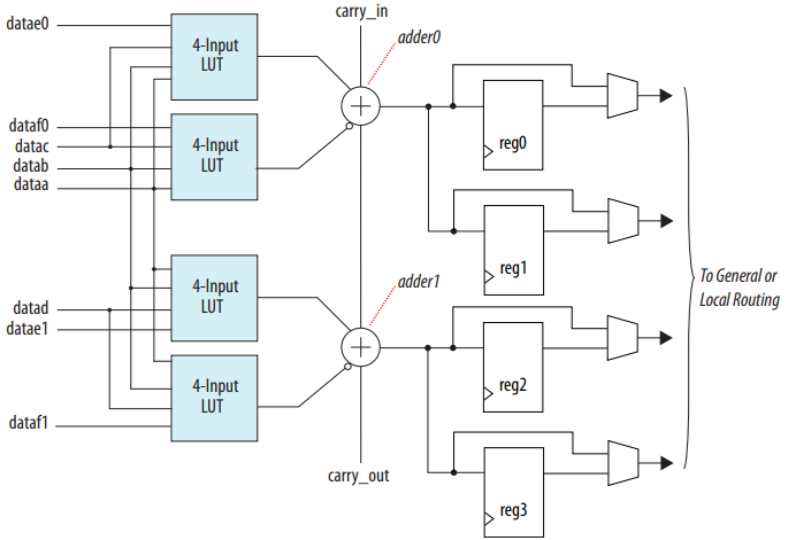
Intel® Cyclone® V ALM Modes

Arithmetic Mode

- The ALM in arithmetic mode uses two sets of two 4-input LUTs along with two dedicated full adders.
- The dedicated adders allow the LUTs to perform pre-adder logic; therefore, each adder can add the output of two 4-input functions.
- The ALM supports simultaneous use of the adder's carry output along with combinational logic outputs. The adder output is ignored in this operation.
- Using the adder with the combinational logic output provides resource savings of up to 50% for functions that can use this mode.

Carry Chain

- The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode.
- The two-bit carry select feature in Arria® V devices halves the propagation delay of carry chains within the ALM. Carry chains can begin in either the first ALM or the fifth ALM in a LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.



source https://www.intel.com/content/www/us/en/docs/programmable/683213/current/arithmetic-mode.html

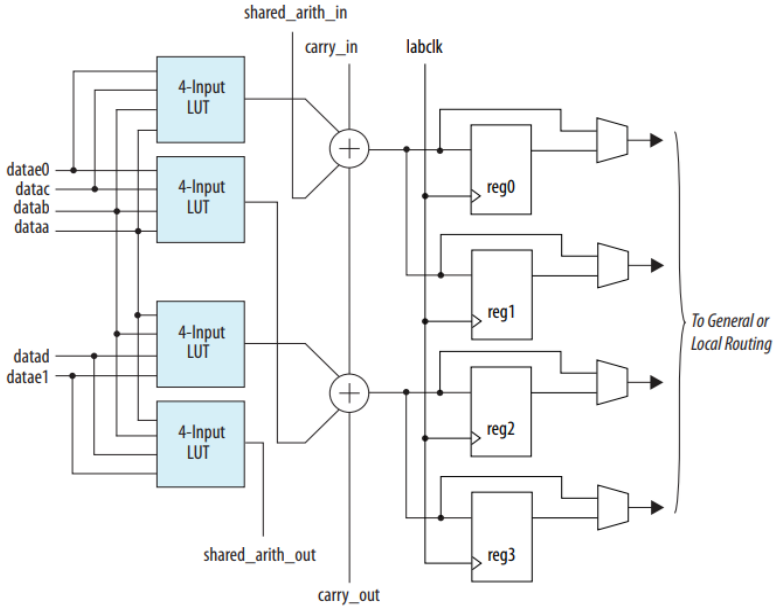
Intel® Cyclone® V ALM Modes

Shared Arithmetic Mode

- The ALM in shared arithmetic mode can implement a 3-input add in the ALM.
- This mode configures the ALM with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder using a dedicated connection called the shared arithmetic chain.

Shared Arithmetic Chain

- The shared arithmetic chain available in enhanced arithmetic mode allows the ALM to implement a 3-input adder. This significantly reduces the resources necessary to implement large adder trees or correlator functions.
- The shared arithmetic chain can begin in either the first or sixth ALM in a LAB.
- Similar to carry chains, the top and bottom half of the shared arithmetic chains in alternate LAB columns can be bypassed. This capability allows the shared arithmetic chain to cascade through half of the ALMs in an LAB while leaving the other half available for narrower fan-in functionality. In every LAB, the column is top-half bypassable; while in MLAB, columns are bottom-half bypassable.

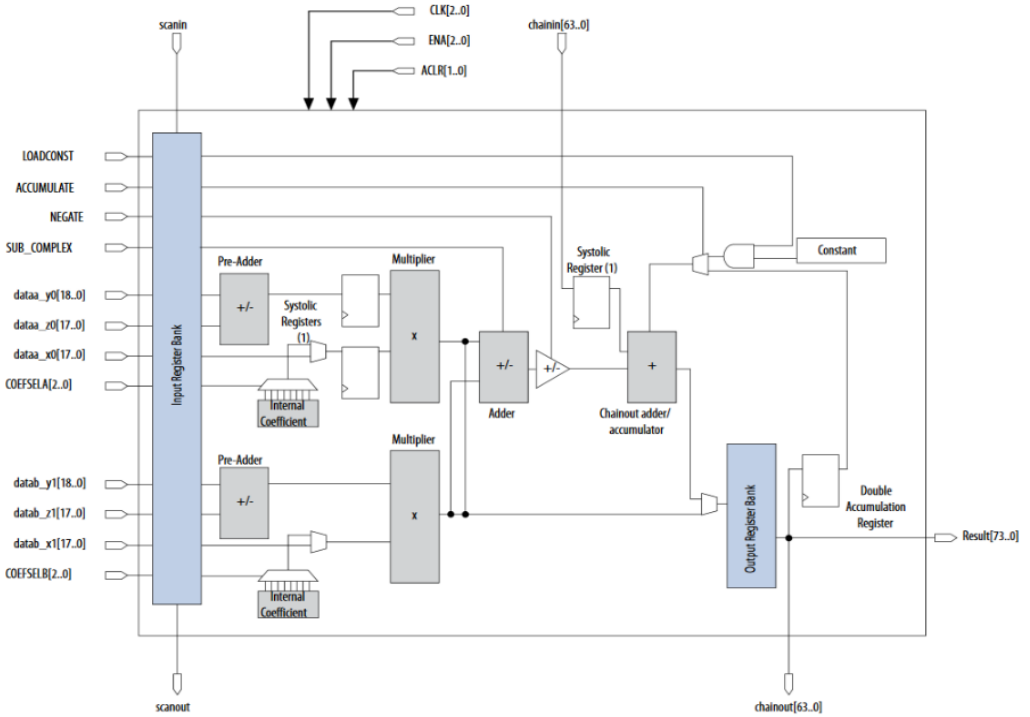


source https://www.intel.com/content/www/us/en/docs/programmable/683213/current/shared-arithmetic-mode.html

Intel® Cyclone® V DSP

The Cyclone V variable precision DSP blocks offer the following features:

- High-performance, power-optimized, and fully registered multiplication operations
- 9-bit, 18-bit, and 27-bit word lengths
- Two 18 x 19 complex multiplications
- Built-in addition, subtraction, and dual 64-bit accumulation unit to combine multiplication results
- Cascading 19-bit or 27-bit to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit, and 27-bit mode for symmetric filters
- Internal coefficient register bank for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder

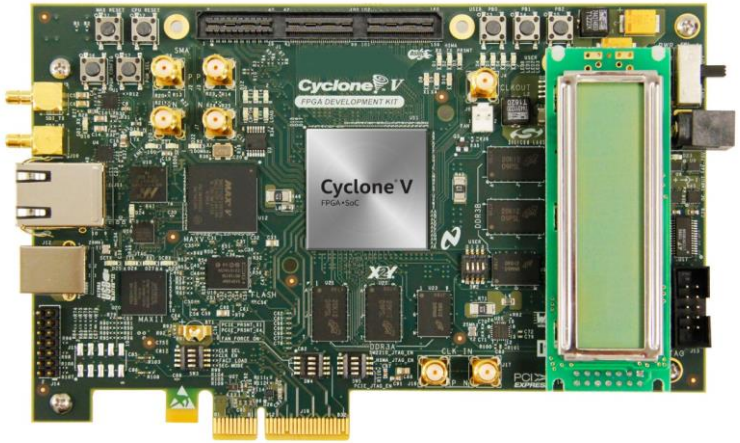


source https://www.intel.com/content/www/us/en/docs/programmable/683375/current/alm-resources.html

https://people.ece.cornell.edu/land/courses/ece5760/DE1_SOC/Cyclone5/DSP_details.PNG

Intel® Cyclone® V Applications

- High-volume applications including protocol bridging, motor control drives, broadcast video converter and capture cards, and handheld devices.
- SoC FPGA lets you reduce system power, system cost, and board space by integrating a HPS – consisting of processors, peripherals, and memory controller,
- Wireless - Mobile backhaul, remote radio heads, picocell
- Automotive - Infotainment, drive assistance, battery management.

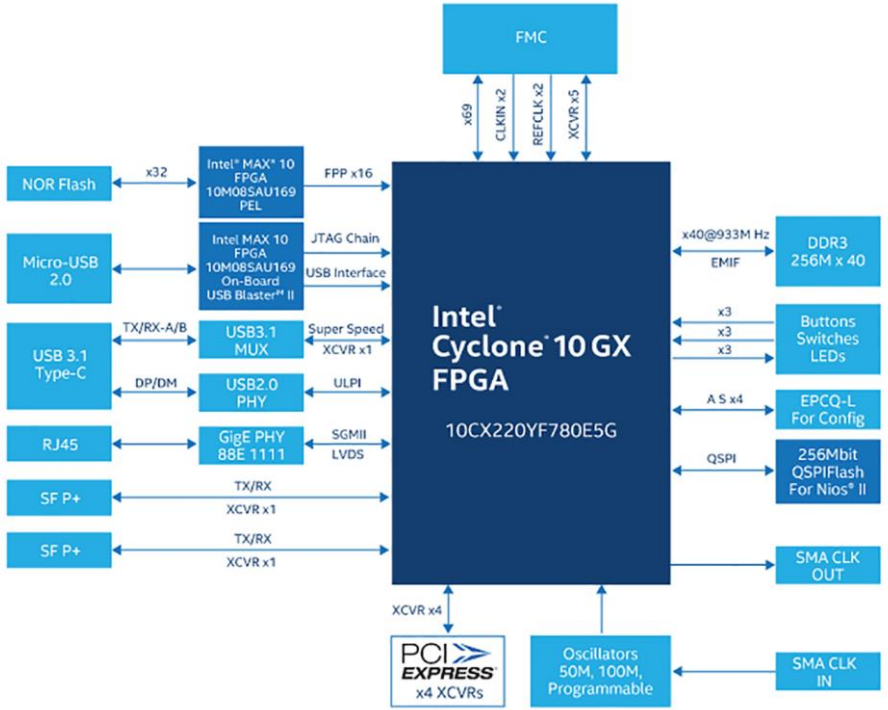


source https://www.intel.com/content/www/us/en/products/details/fpga/cyclone/v.html

Intel® Cyclone® 10 GX

Digital Logic Design with FPGA

- The Intel® Cyclone® 10 GX device family consists of high-performance and power-efficient 20 nm low cost FPGAs.
- Intel® Cyclone® 10 GX device family delivers higher core, transceiver, and I/O performance than the previous generation of low cost FPGAs.
- The Intel® Cyclone® 10 GX devices are ideal for high bandwidth, low-cost applications in diverse markets.
- Used in applications such as:
  - Machine vision
  - Robotics
  - Programmable logic controller and drivers
- Family was launched in 2017.



source https://www.intel.com/content/www/us/en/docs/programmable/683485/current/device-overview.html

https://www.intel.com/content/www/us/en/products/details/fpga/development-kits/cyclone/10-gx.html

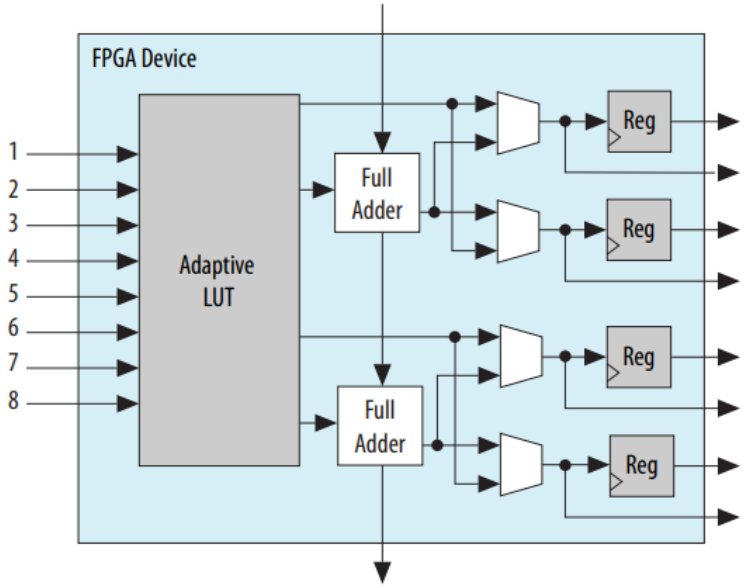
Intel® Cyclone® 10 GX

	PRODUCT LINE	10CX085	10CX105	10CX150	10CX220
Resources	Logic elements (LEs)[1]	85,000	104,000	150,000	220,000
	Adaptive logic modules (ALMs)	31,000	38,000	54,770	80,330
	ALM registers	124,000	152,000	219,080	321,320
	M20K memory blocks	291	382	475	587
	M20K memory size (Kb)	5,820	7,640	9,500	11,740
	MLAB memory size (Kb)	653	799	1,152	1,690
	Variable-precision digital signal processing (DSP) blocks	84	125	156	192
	18 x 19 multipliers	168	250	312	384
	Peak fixed-point peformance (GMACS)[2]	151	225	281	346
	Peak floating-point performance (GFLOPS)[3]	59	88	109	134
I/O and Architectural Features	Global clock networks	32	32	32	32
	Regional clocks	8	8	8	8
	Maximum user I/O pins	192	284	284	284
	Maximum LVDS pairs 1.4 Gbps (RX or TX)	72	118	118	118
	Maximum transceiver count (12.5 Gbps)	6	12	12	12
	Maximum 3V I/O pins	48	48	48	48
	PCI Express* (PCIe*) hard IP blocks (Gen2 x4)[4]	1	1	1	1
	Memory devices supported	DDR3, DDR3L, LPDDR3			

source https://www.intel.com/content/www/us/en/content-details/714179/intel-cyclone-10-gx-fpgas-family-overview-product-table.html

Intel® Cyclone® 10 GX ALM

- Intel Cyclone 10 GX devices use a 20 nm ALM as the basic building block of the logic fabric.
- The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.
- The ALM uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.



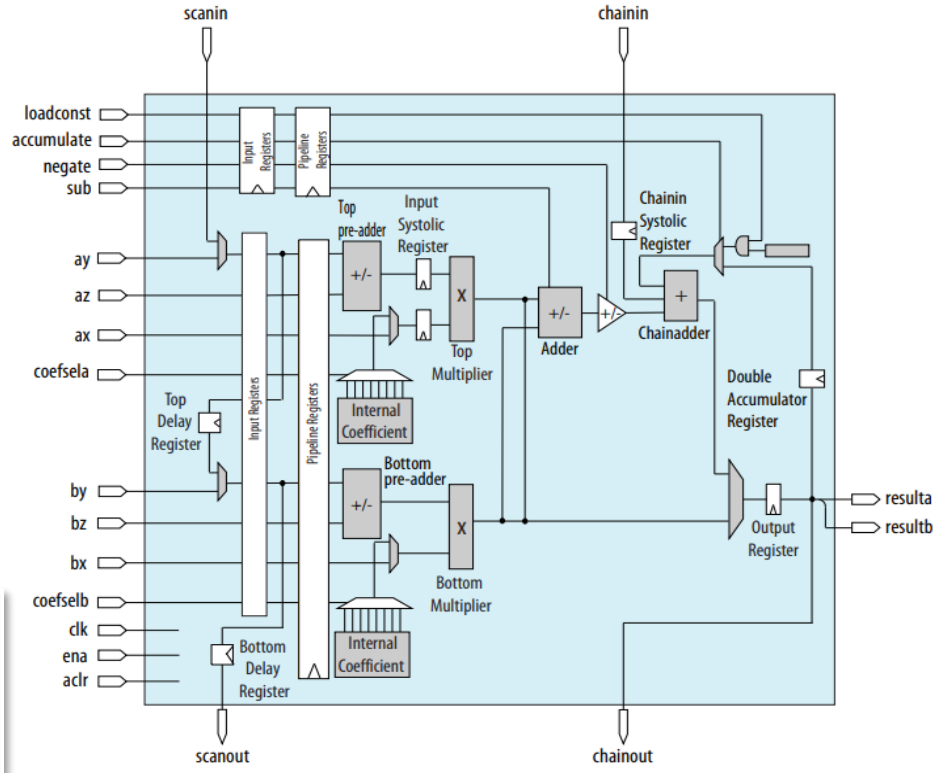
source https://www.intel.com/content/www/us/en/docs/programmable/683485/current/adaptive-logic-module.html

Intel® Cyclone® 10 GX DSP

Digital Logic Design with FPGA

- High-performance, power-optimized, and fully registered multiplication operations
- 8-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications

Usage Example	Multiplier Size (Bit)	DSP Block Resources
Medium precision fixed point	Two 18 x 19	1
High precision fixed or Single precision floating point	One 27 x 27	1
Fixed point FFTs	One 19 x 36 with external adder	1
Very high precision fixed point	One 36 x 36 with external adder	2
Double precision floating point	One 54 x 54 with external adder	4



source https://www.intel.com/content/www/us/en/docs/programmable/683485/current/variable-precision-dsp-block.html

Intel® Cyclone® 10 GX Applications

- Embedded Video and Image Processing Applications - JPEG XS compression can be used in applications that previously transported uncompressed image and video data – enabling systems to offer higher quality resolution at faster frame rates.
- Easy Machine Vision Camera (EasyMVC) is designed to eliminate the hurdles of machine vision system development.

source https://www.intel.com/content/www/us/en/products/details/fpga/cyclone/10/gx.html

Intel® Cyclone® 10 LP

- The Intel® Intel® Cyclone® 10 LP FPGAs are optimized for low cost and low static power, making them ideal for high-volume and cost-sensitive applications.
- Intel® Cyclone® 10 LP devices provide a high density sea of programmable gates, on-board resources, and general purpose I/Os. These resources satisfies the requirements of I/O expansion and chip-to-chip interfacing. The Intel® Cyclone® 10 LP architecture suits smart and connected end applications across many market segments:
    - Industrial and automotive
    - Broadcast, wireline, and wireless
    - Compute and storage
    - Government, military, and aerospace
    - Medical, consumer, and smart energy
- Family was launched in 2017

source https://www.intel.com/content/www/us/en/docs/programmable/683879/current/device-overview.html

https://www.intel.com/content/www/us/en/products/details/fpga/development-kits/cyclone/10-lp-evaluation-kit.html

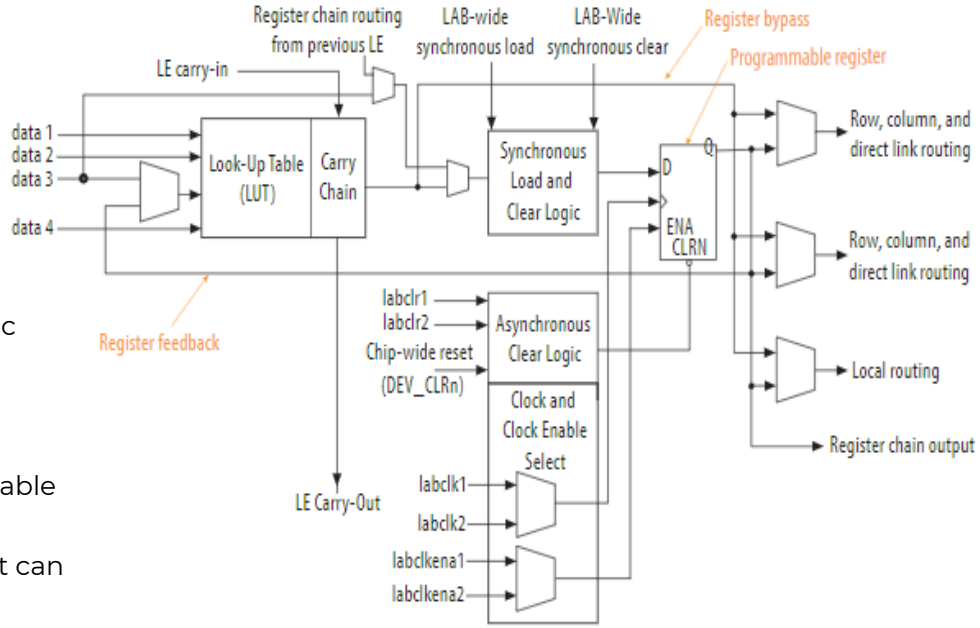
Intel® Cyclone® 10 LP

PRODUCT LINE		10CL006	10CL010	10CL016	10CL025	10CL040	10CL055	10CL080	10CL120
Resources	Logic elements (LEs)[1]	6,000	10,000	16,000	25,000	40,000	55,000	80,000	120,000
	M9K memory blocks	30	46	56	66	126	260	305	432
	M9K memory size (Kb)	270	414	504	594	1,134	2,340	2,745	3,888
	DSP Blocks (18 x 18 multipliers)	15	23	56	66	126	156	244	288
	Phase-locked loops (PLL)	2	2	4	4	4	4	4	4
I/O and Architectural Features	Global clock networks	10	10	20	20	20	20	20	20
	Maximum user I/O pins	176	176	340	150	325	321	423	525
	Maximum LVDS channels	65	65	137	52	124	132	178	230

Digital

source https://www.intel.com/content/www/us/en/content-details/714190/intel-cyclone-10-lp-fpgas-family-overview-product-table.html?wapkw=cyclone%2010%20gx%20product%20table

Intel® Cyclone® 10 LP Logic Elements

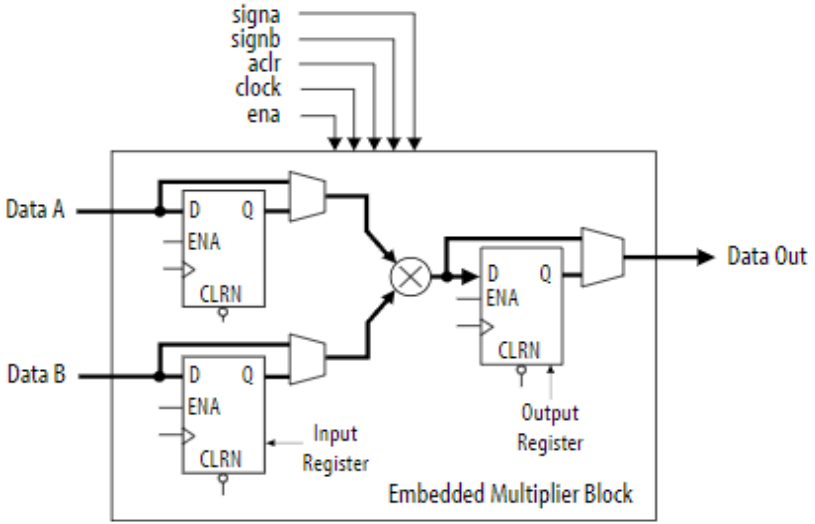


- The LAB (Logic Array Blocks) consists of 16 logic elements (LE) and a LAB-wide control block.
- An LE is the smallest unit of logic in the Intel® Cyclone® 10 LP device architecture.
- Each LE has four inputs, a four-input look-up table (LUT), a register, and output logic.
- The four-input LUT is a function generator that can implement any function with four variables.

source https://www.intel.com/content/www/us/en/docs/programmable/683879/current/logic-elements-and-logic-array-blocks.html

Intel® Cyclone® 10 LP DSP

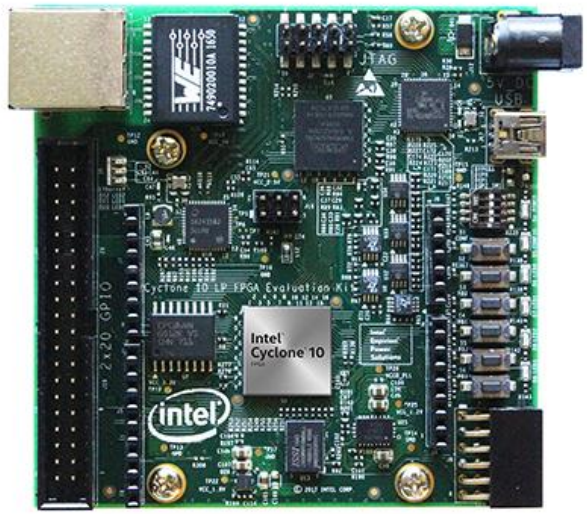
- Each embedded multiplier block in Intel Cyclone 10 LP devices supports one individual 18 × 18-bit multiplier or two individual 9 × 9-bit multipliers.
- You can cascade the multiplier blocks to form wider or deeper logic structures.
- There are some DSP IPs for Intel® Cyclone® 10 LP devices, including:
    - Finite impulse response (FIR)
    - Fast Fourier transform (FFT)
    - Numerically controlled oscillator (NCO) functions



source https://www.intel.com/content/www/us/en/docs/programmable/683879/current/embedded-multipliers.html

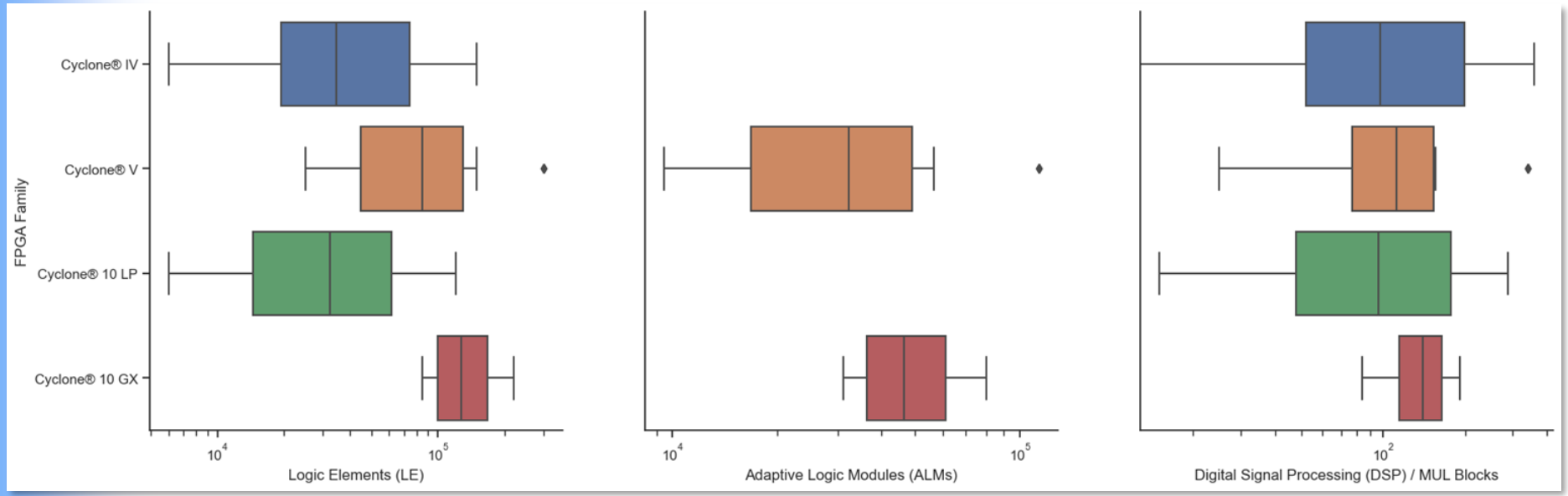
Intel® Cyclone® 10 LP Applications

- Chip-to-Chip Interfacing - image pipeline processing for real-time applications that need high frame rates, low latency, and high-processing throughput.
- Motor Control - devices support a wide variety of industrial Ethernet protocols and are leveraged to implement pulse width modulator (PWM) and encoder interfaces, which when repeated multiple times in parallel, allows for multi-axis control.

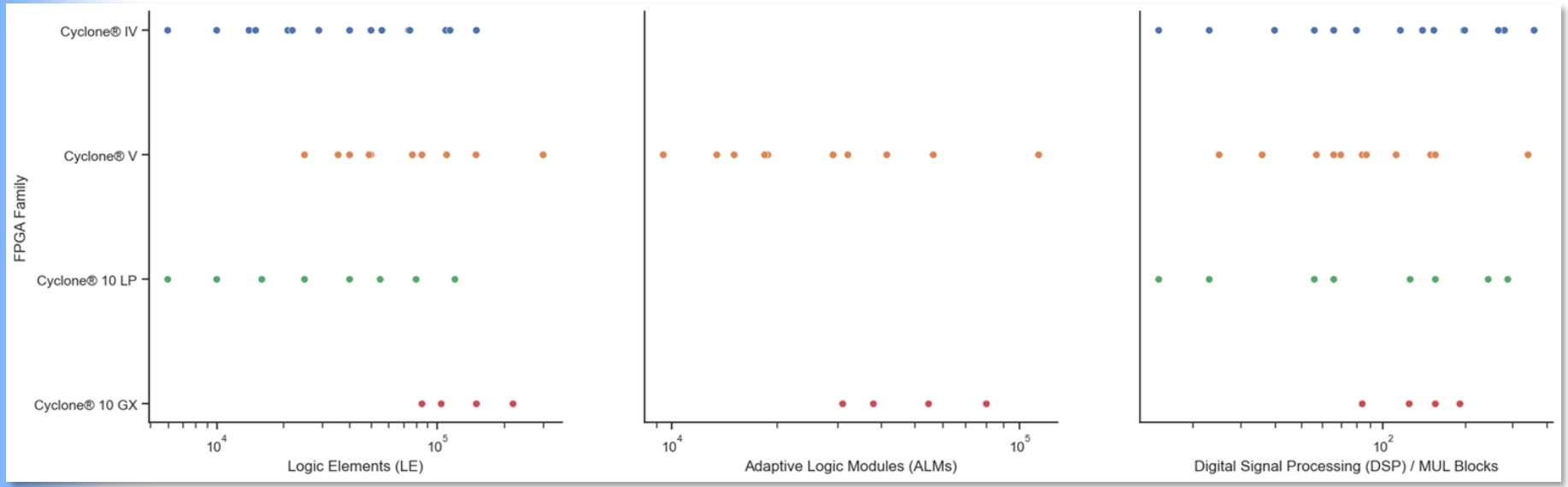


source https://www.intel.com/content/www/us/en/products/details/fpga/cyclone/10/lp.html

Intel® Cyclone® Family Differences

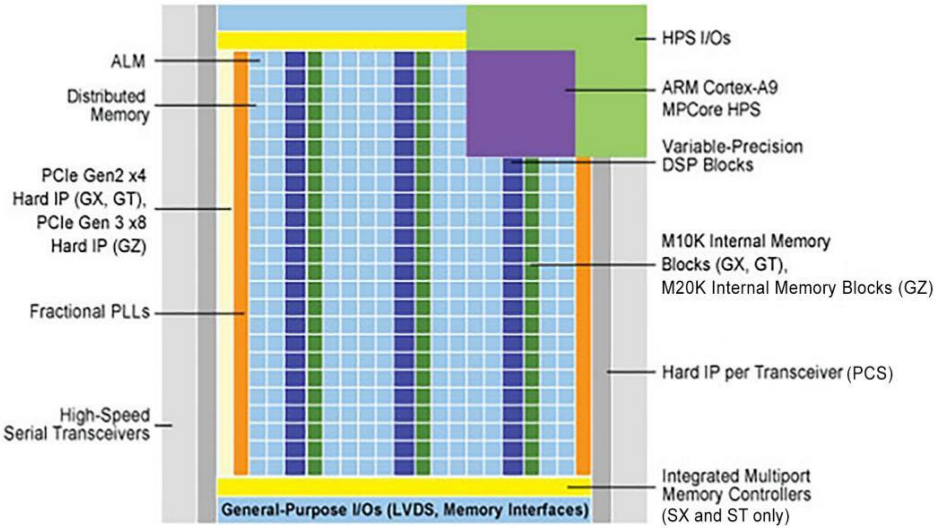


Intel® Cyclone® Family Differences



Intel® Arria® Series

- Preserve the flexibility of processor boot / FPGA configuration sequence, system response to processor reset, and independent memory interfaces of a two-chip solution.
- Maintain data integrity and reliability with integrated ECC.
- Protect DRAM memory shared by the processor and FPGA with an integrated memory protection unit.
- Enable system-level debug with Intel's FPGA-adaptive debugging for unmatched visibility and control of the whole device.



source https://www.intel.com/content/www/us/en/products/details/fpga/arria/v.html

Intel® Arria® V Series

- The Arria® V FPGA family offers the highest bandwidth and delivers the lowest total power for midrange applications, such as remote radio units, 10G/40G line cards, and broadcast studio equipment.
- There are five targeted variants, including SoC variants with a dual-core ARM* Cortex*-A9 hard processor system (HPS) to best meet your performance, power, and integration needs.
- Family was launched in 2011.

source https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/item.html

Intel® Arria® V Series Family

Arria® V GZ FPGA
- Offers the lowest power-per-bandwidth for midrange applications, and are ideal for power-sensitive designs that require transceivers up to 12.5 Gbps.

Arria® V GT FPGA
- Offers the lowest total power for mid-range applications and the lowest power transceivers for speeds up to 10.3125 Gbps.

Arria® V GX FPGA
- Offers the lowest total power for mid-range applications and the lowest power transceivers for speeds up to 10.3125 Gbps.

Arria® V ST SoC FPGA
- Intel® SoC FPGA with ARM*-based HPS and 10.3125 Gbps transceivers.

Arria® V SX SoC FPGA
- Intel® SoC FPGA with ARM*-based HPS and 6.5536 Gbps backplane-capable transceivers.

source https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/item.html

Intel® Arria® V Series

	Product Line	Arria V GX FPGAs[1]								Arria V GT FPGAs[1]				Arria V GZ FPGAs[1]				Arria V SX SoCs[1]		Arria V ST SoCs[1]	
		5AGXA1	5AGXA3	5AGXA5	5AGXA7	5AGXB1	5AGXB3	5AGXB5	5AGXB7	5AGTC3	5AGTC7	5AGTD3	5AGTD7	5AGZE1	5AGZE3	5AGZE5	5AGZE7	5ASXB3	5ASXB5	5ASTD3	5ASTD5
Resources	LEs (K)	75	156	190	242	300	362	420	504	156	242	362	504	220	360	400	450	350	462	350	462
	ALMs	28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240	58,900	91,680	136,880	190,240	83,020	135,840	150,960	169,800	132,075	174,340	132,075	174,340
	Registers	113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960	235,600	366,720	547,520	760,960	332,080	543,360	603,840	679,200	528,300	697,360	528,300	697,360
	M10K memory blocks	800	1,051	1,180	1,366	1,510	1,726	2,054	2,414	1,051	1,366	1,726	2,414	–	–	–	–	1,729	2,282	1,729	2,282
	M20K memory blocks	–	–	–	–	–	–	–	–	–	–	–	–	585	957	1,440	1,700	–	–	–	–
	M10K memory (Kb)	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140	10,510	13,660	17,260	24,140	–	–	–	–	17,290	22,820	17,290	22,820
	M20K memory (Kb)	–	–	–	–	–	–	–	–	–	–	–	–	11,700	19,140	28,800	34,000	–	–	–	–
	MLAB memory (Kb)	463	961	1,173	1,448	1,852	2,098	2,532	2,906	961	1,448	2,098	2,906	2,594	4,245	4,718	5,306	2,014	2,658	2,014	2,658
	Variable-precision DSP blocks	240	396	600	800	920	1,045	1,092	1,156	396	800	1,045	1,156	800	1,044	1,092	1,139	809	1,090	809	1,090
	18 x 18 multipliers	480	792	1,200	1,600	1,840	2,090	2,184	2,312	792	1,600	2,090	2,312	1,600	2,088	2,184	2,278	1,618	2,180	1,618	2,180
Clocks, Maximum I/O Pins, and Architectural Features	Processor cores (ARM Cortex-A9)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	Dual	Dual	Dual	Dual
	Maximum CPU clock frequency (GHz)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1.05[2]	1.05[2]	1.05[2]	1.05[2]
	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
	PLLs[3] (FPGA)	10	10	12	12	12	12	16	16	10	12	12	16	20	20	24	24	14	14	14	14
	PLLs (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	3	3	3	3
	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3[4]																			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12																			
	LVDS channels (receiver/transmitter)	80/67	80/67	136/120	136/120	176,160	176,160	176,160	176,160	80/70	136/120	176/160	176/160	108/99	108/99	168/166	168/166	120/136	120/136	120/136	120/136
	Transceiver count (6.5536 Gbps)	9	9	24	24	24	24	36	36	3	6	6	6	–	–	–	–	30	30	30	30
	Transceiver count (10.3125 Gbps)[5]	–	–	–	–	–	–	–	–	4	12	12	20	–	–	–	–	–	–	16	16
	Transceiver count (12.5 Gbps)	–	–	–	–	–	–	–	–	–	–	–	–	24	24	36	36	–	–	–	–
	PCIe hard IP blocks (Gen2 x4)	1	1	2	2	2	2	2	2	1	2	2	2	–	–	–	–	2	2	2	2
	PCIe hard IP blocks (Gen2 x8, Gen3)	–	–	–	–	–	–	–	–	–	–	–	–	1	1	1	1	–	–	–	–
	GPIOs (FPGA)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	540	540	540	540
	GPIOs (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	208	208	208	208
	Hard memory controllers[6] (FPGA)	2	2	4	4	4	4	4	4	2	4	4	4	–	–	–	–	3	3	3	3
	Hard memory controllers (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	1	1	1
	Memory devices supported	DDR3, DDR2, DDR II+[7], QDR II, QDR II+, RLDRAM II, RLDRAM 3[8], LPDDR[7], LPDDR2[7]																			

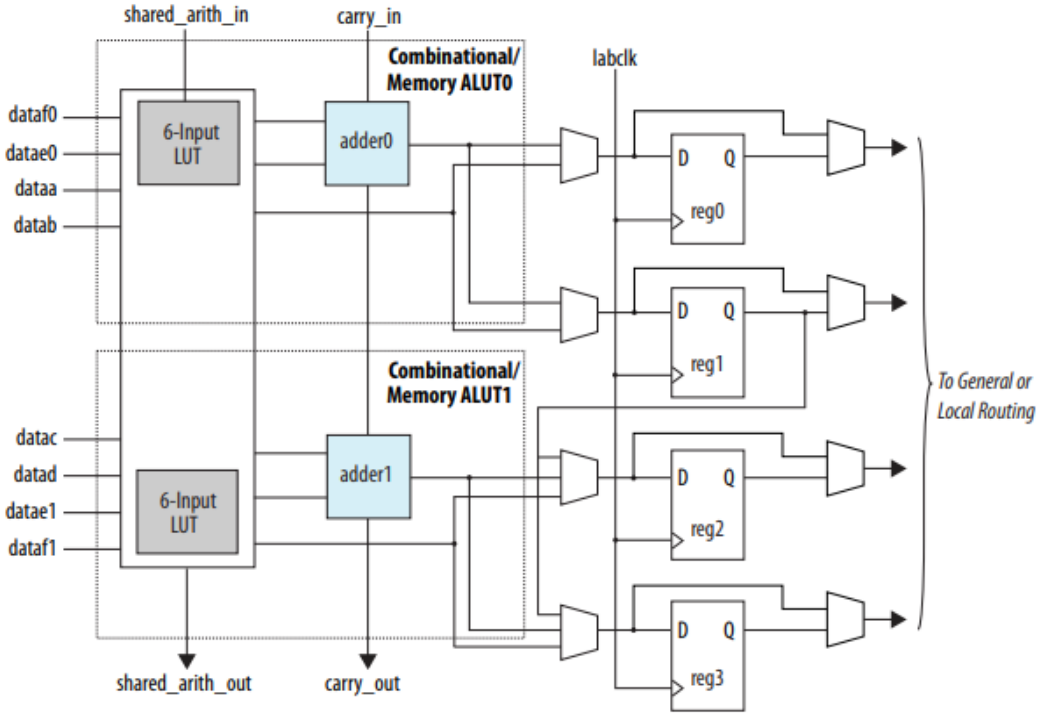
source https://www.intel.com/content/www/us/en/content-details/714173/arria-v-fpga-family-overview-product-table.html

Intel® Arria® V ALM

- The Arria V ALM operates in any of the following modes:
  - Normal mode
  - Extended LUT mode
  - Arithmetic mode
  - Shared arithmetic mode
- One ALM contains four programmable registers. Each register has the following ports:
  - Data
  - Clock
  - Synchronous and asynchronous clear
  - Synchronous load
- For combinational functions, the registers are bypassed and the output of the look-up table (LUT) drives directly to the outputs of an ALM.
- The general routing outputs in each ALM drive the local, row, and column routing resources. Two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources.
- The LUT, adder, or register output can drive the ALM outputs. The LUT or adder can drive one output while the register drives another output.

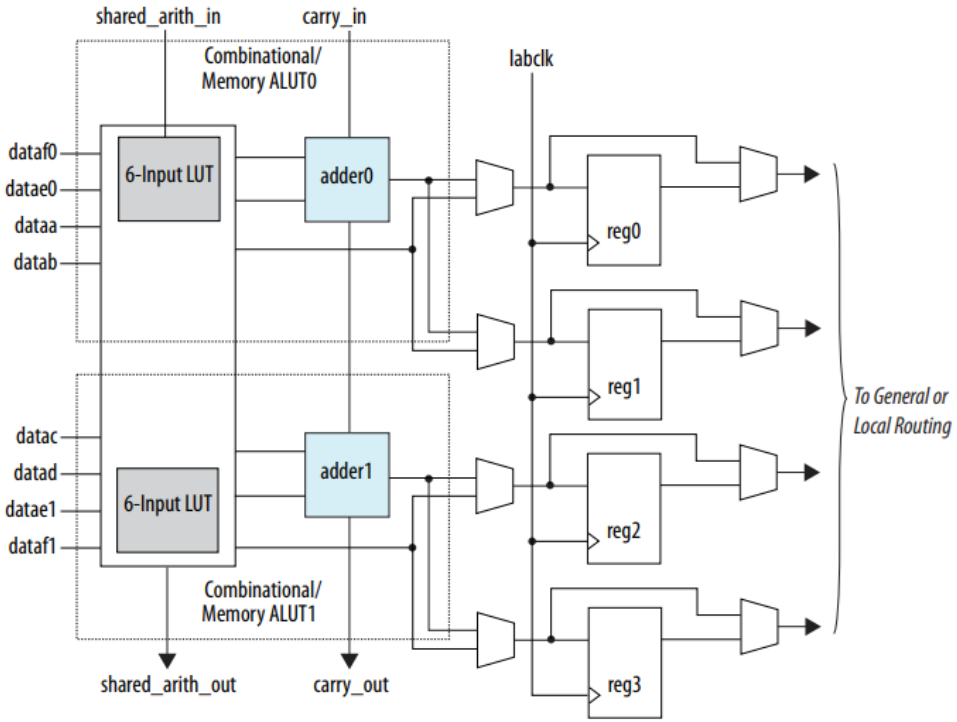
source https://www.intel.com/content/www/us/en/docs/programmable/683213/current/logic-array-blocks-and-adaptive-logic-24877.html

Intel® Arria® V GX, GT, SX and ST ALM



source https://www.intel.com/content/www/us/en/docs/programmable/683213/current/logic-array-blocks-and-adaptive-logic-24877.html

Intel® Arria® V GZ ALM

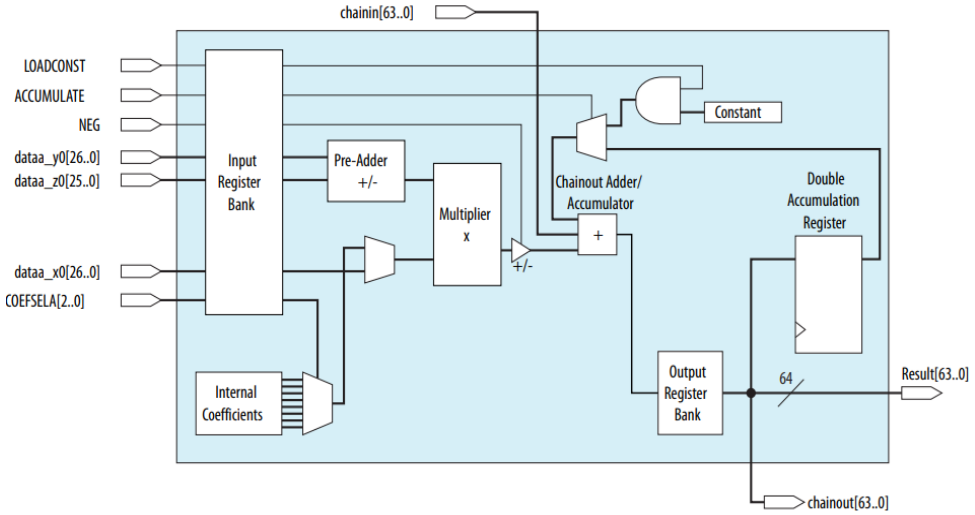


source https://www.intel.com/content/www/us/en/docs/programmable/683213/current/logic-array-blocks-and-adaptive-logic-24877.html

Intel® Arria® V DSP

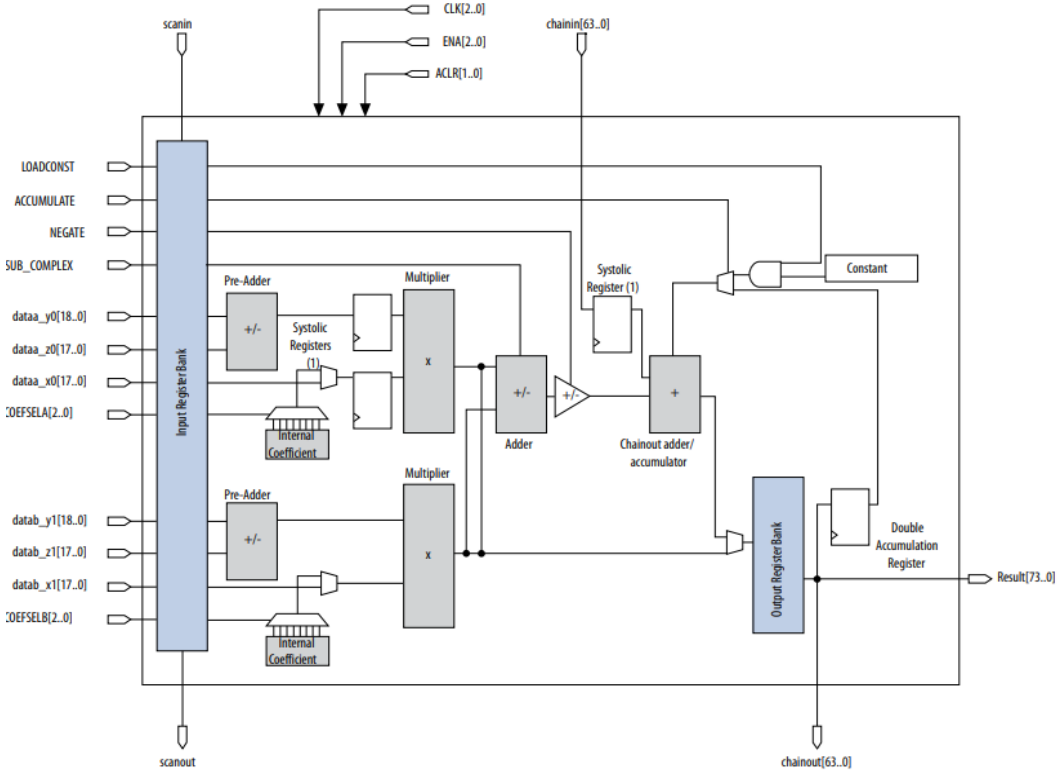
The Arria V variable precision DSP blocks offer the following features:

- High-performance, power-optimized, and fully registered multiplication operations
- 9-bit, 18-bit, 27-bit, and 36-bit(2) word lengths
- 18 x 19 and 18 x 25 complex multiplications (2)
- Built-in addition, subtraction, and 64-bit accumulation unit to combine multiplication results
- Cascading 19-bit or 27-bit to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 18-bit, 19-bit, and 27-bit mode for symmetric filters
- Internal coefficient register bank for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder



source https://www.intel.com/content/www/us/en/docs/programmable/683213/current/features.html

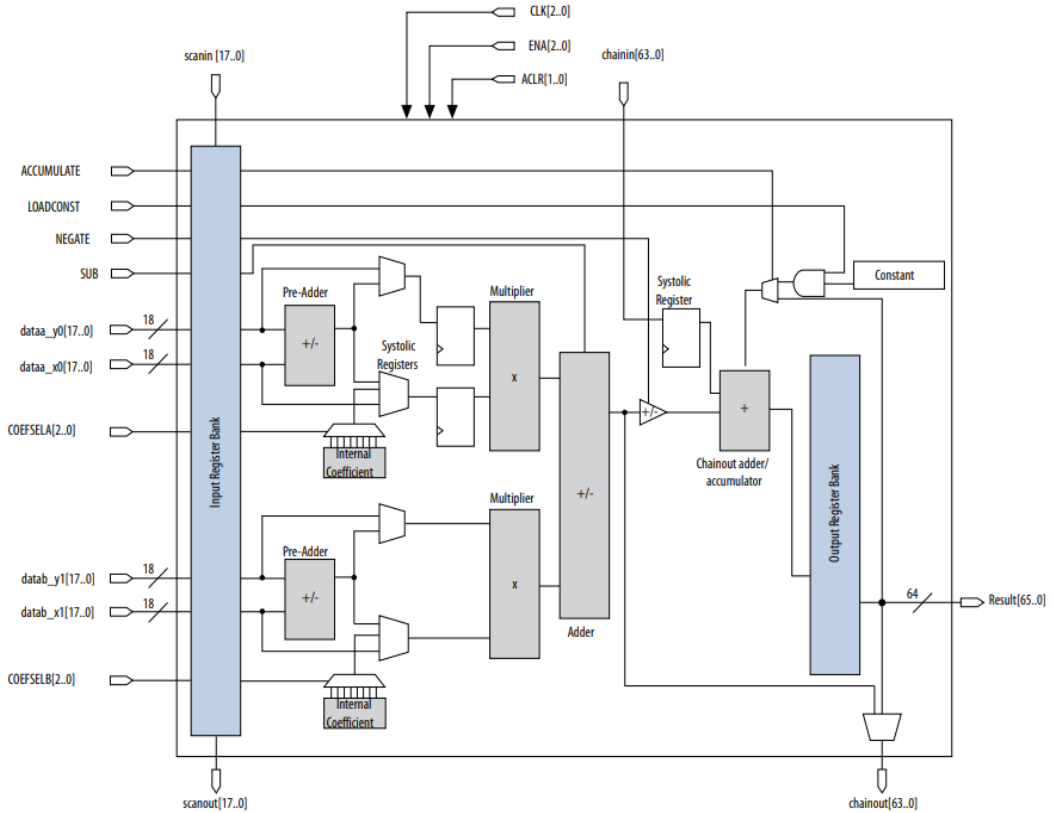
Intel® Arria® V GX, GT, SX and ST DSP



Note:
1. When enabled, systolic registers are clocked with the same clock source as the output register bank.

source https://www.intel.com/content/www/us/en/docs/programmable/683213/current/features.html

Intel® Arria® V GZ DSP



source https://www.intel.com/content/www/us/en/docs/programmable/683213/current/features.html

Intel® Arria® V Applications

Wireless Communications

- Remote radioheads, RF cards and channel cards, Mobile backhaul.

Wireline Communications

- 20G/40G bridging and switching, 20G packet processing, Gigabit-capable passive optical network (GPON).

Broadcast

- Digital modulation equipment (including EdgeQAM and satellite and terrestrial broadcast), Pro audio/visual (A/V) switches, Video conferencing, PCIe capture and cameras.

Computer & Storage

- Custom storage, Flash memory cache, Plug-in cards.

Military

- Guidance control, Tactical electronic warfare, Custom storage, Electro-optical/infrared (OR/IR) systems.

Test & Medical

- Ultrasound, CT scanning, Other diagnostic imaging, Portable and wireless tests.

Industrial & Consumer

- Human-machine interface, I/O companion, High-end display, High-end video surveillance.

source https://www.intel.com/content/www/us/en/products/details/fpga/arria/v.html

Intel® Arria® 10 Series

- Intel® Arria® 10 FPGA and Soc FPGA delivers more than a speed grade faster core performance and up to a 20% fMAX advantage compared to the competition, using publicly-available OpenCore designs, and up to 40 percent lower power than previous generation FPGA and SoC FPGA.
- Intel® Arria® 10 FPGA and Soc FPGA delivers optimal performance, power efficiency and small form factor are ideal for a broad array of applications such as communications, data center, military, broadcast, automotive, and other FPGA midrange applications.
- Family was launched in 2013.

source https://www.intel.com/content/www/us/en/products/details/fpga/arria/10/gt.html

Intel® Arria® 10 Series

Intel® Arria® 10 GT FPGA

- High-speed interconnect capability of the device makes it an ideal choice for projects requiring superior data transfer speed.
- This device offers the power-, space-, and cost-efficient integration of video and image processing including 4K, 3D, and CODECs for the shortest time-to-market for production studio equipment.
- Reduce power and cost for networking and telecommunications applications.

Intel® Arria® 10 GX FPGA

- This device provides a vast playground with over 1 million logic elements (LEs).
- Programmable power technology reduces power demand while maintaining top performance.
- This device can be used in similar applications where the Arria 10 GT is used.

Intel® Arria® 10 SX SoC FPGA

- SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.
- Well-suited for broadcast applications requiring high performance and flexibility, offering versatility in managing logic functions such as video format conversion, audio processing and efficient link management.
- Develop flexible, multi-mission RADAR, or 'FlexDAR' capabilities.

source https://www.intel.com/content/www/us/en/products/details/fpga/arria/10/gt.html
https://www.intel.com/content/www/us/en/products/details/fpga/arria/10/gx.html
https://www.intel.com/content/www/us/en/products/details/fpga/arria/10/sx.html

Intel® Arria® 10 Series

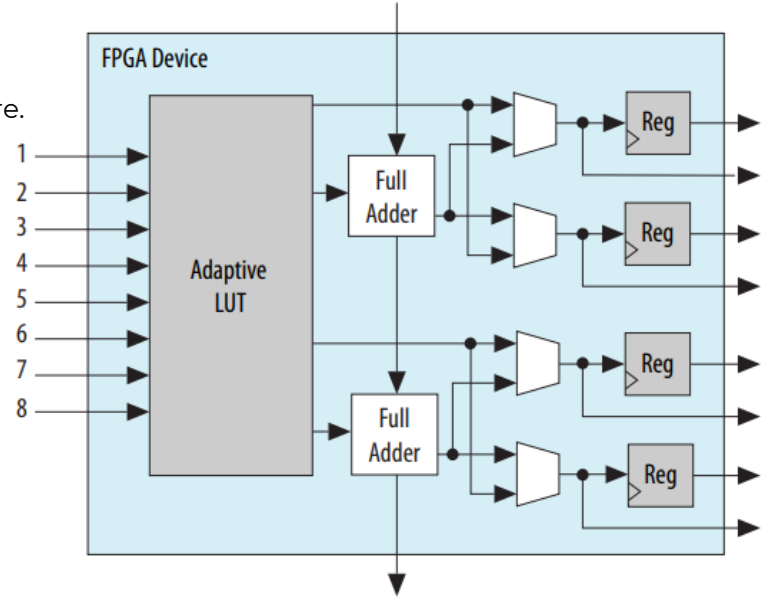
Digital Logic Design with FPGA

PRODUCT LINE		GX 160 SX 160	GX 220 SX 220	GX 270 SX 270	GX 320 SX 320	GX 480 SX 480	GX 570 SX 570	GX 660 SX 660	GX 900	GX 1150	GT 900	GT 1150
Resources	LEs (K)	160	220	270	320	480	570	660	900	1,150	900	1,150
	System logic elements (K)	210	288	354	419	629	747	865	1,180	1,506	1,180	1,506
	Adaptive logic modules (ALMs)	61,510	83,730	101,620	118,730	181,790	217,080	250,540	339,620	427,200	339,620	427,200
	Registers	246,040	334,920	406,480	474,920	727,160	868,320	1,002,160	1,358,480	1,708,800	1,358,480	1,708,800
	M20K memory blocks	440	588	750	891	1,438	1,800	2,133	2,423	2,713	2,423	2,713
	M20K memory (Mb)	9	11	15	17	28	35	42	47	53	47	53
	MLAB memory (Mb)	1.0	1.8	2.4	2.8	4.3	5.0	5.7	9.2	12.7	9.2	12.7
	Hardened single-precision floating-point multipliers/adders	156/156	191/191	830/830	985/985	1,368/1,368	1,523/1,523	1,688/1,688	1,518/1,518	1,518/1,518	1,518/1,518	1,518/1,518
	18 x 19 multipliers	312	382	1,660	1,970	2,736	3,046	3,376	3,036	3,036	3,036	3,036
	Peak fixed-point performance (GMACS)[1]	343	420	1,826	2,167	3,010	3,351	3,714	3,340	3,340	3,340	3,340
	Peak floating-point performance (GFLOPS)	140	172	747	887	1,231	1,371	1,519	1,366	1,366	1,366	1,366
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	32	32	32	32	32	32	32	32	32	32	32
	Regional clocks	8	8	8	8	8	8	16	16	16	16	16
	Hard processor system (available in SX devices only)	Dual-core Arm* Cortex*-A9 MPCore* processor. See the following page for details.							–			
	Maximum LVDS channels (1.6 G)	120	120	168	168	222	324	270	384	384	312	312
	Maximum user I/O pins	288	288	384	384	492	696	696	768	768	624	624
	Transceiver count (17.4 Gbps)	12	12	24	24	36	48	48	96	96	72	72
	Transceiver count (25.78 Gbps)	–	–	–	–	–	–	–	–	–	6	6
	PCIe* hardened IP blocks (Gen3 x8)[2]	1	1	2	2	2	2	2	4	4	4	4
	Maximum 3 V I/O pins	48	48	48	48	48	96	96	–	–	–	–

source https://www.intel.com/content/www/us/en/content-details/714167/intel-arria-10-fpga-and-soc-fpga-family-overview-product-table.html?DocID=714167

Intel® Arria® 10 ALM

- Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.
- The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations
- Uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.



source https://www.intel.com/content/www/us/en/docs/programmable/683332/current/adaptive-logic-module.html

Intel® Arria® 10 DSP

- The Intel Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.
- Features for fixed-point arithmetic:
  - High-performance, power-optimized, and fully registered multiplication operations
  - 18-bit and 27-bit word lengths
  - Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
  - Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
  - Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
  - Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
  - And some other features
- Features for floating-point arithmetic:
  - A completely hardened architecture that supports multiplication, addition, subtraction, multiply-add, and multiply-subtract
  - Multiplication with accumulation capability and a dynamic accumulator reset control
  - Multiplication with cascade summation capability
  - Multiplication with cascade subtraction capability
  - Complex multiplication
  - Direct vector dot product
  - Systolic FIR filter

source https://www.intel.com/content/www/us/en/docs/programmable/683332/current/variable-precision-dsp-block.html

Intel® Arria® 10 Applications

20x10G Optical Transpor

- Reduce power and cost when using Nx10G and Nx100G transmission equipment for networking and telecommunications applications. Up to 53Mb RAM, built-in 10G/40G error correction, and broad protocol support boost your product's networking abilities: switching, security, monitoring, self-testing, and traffic management.

Broadcast and Professional Audio-Visual Equipment

- This device offers the power-, space-, and cost-efficient integration of video and image processing including 4K, 3D, and CODECs for the shortest time-to-market for production studio equipment.

Military RADAR/FlexDar

- Develop flexible, multi-mission RADAR, or 'FlexDAR' capabilities.

Cloud Servers and Storage

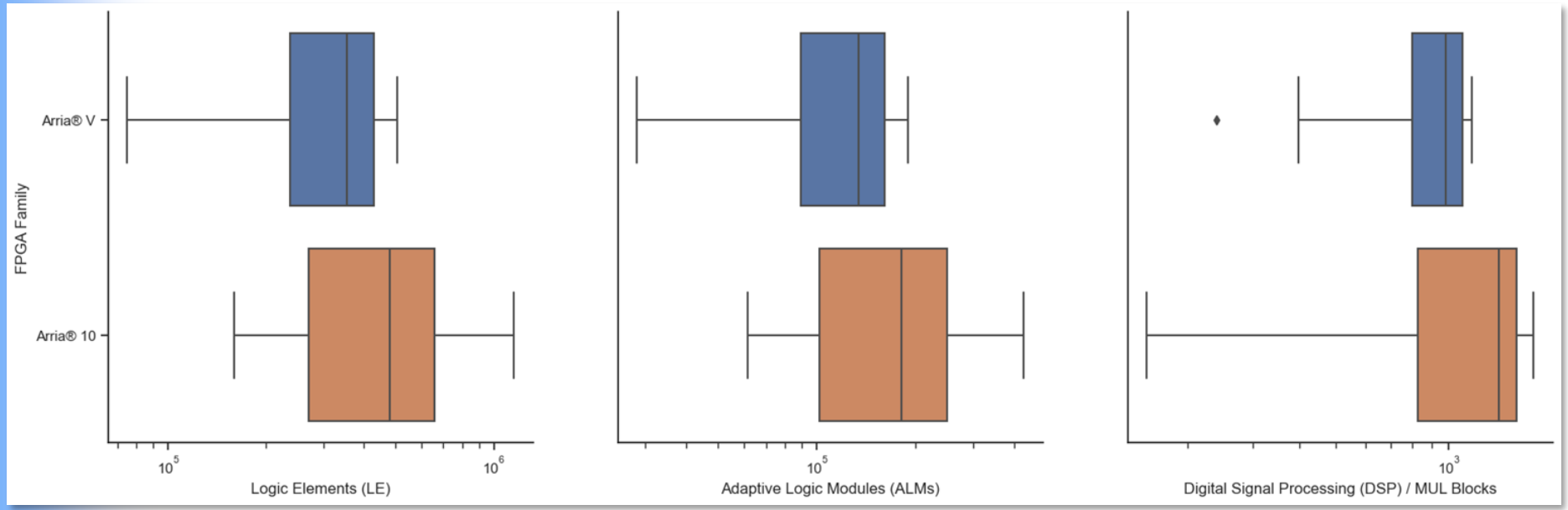
- Efficiently perform logic functions such as flash cache processing, acceleration, and SATA/SAS, as well as processor functions like flash cache control, host offload, and co-processing.

High-Performance Broadcast Infrastructure

- This FPGA is well-suited for broadcast applications requiring high performance and flexibility, offering versatility in managing logic functions such as video format conversion, multiplexing, switching, and bridging, alongside proficiently handling processor tasks like audio processing, video compression, and efficient link management.

source https://www.intel.com/content/www/us/en/products/details/fpga/arria/10/gx.html

Intel® Arria® Differences



Intel® Arria® Differences