Digital Logic
Design with FPGA

Intel FPGA Architectures

Device and Products (2)

Intel® Stratix® Series

- First FPGA devices to support Intel® Ultra Path Interconnect (UPI) for direct coherent connection to Intel® Xeon® Scalable processor.
- FPGA PCIe* hard IP with configuration up to Gen4 x16 at 16 Gbps.
- Intel® Hyperflex™ FPGA Architecture delivers up to 1 GHz performance, enabling breakthroughs in computational throughput.
- Hardened single-precision floating-point DSP block, compliant with IEEE 754 standard, delivers GPU-class floating performance at a fraction of the power.
- Hardened AI Tensor Block tuned for common matrix-matrix or vector-matrix multiplications in AI acceleration applications resulting in up to 143 INT8 TOPS or 286 INT4 TOPS.3
- Secure cloud solutions using the security features.

source https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/item.html

Stratix® Series Ultra Path Interconnect

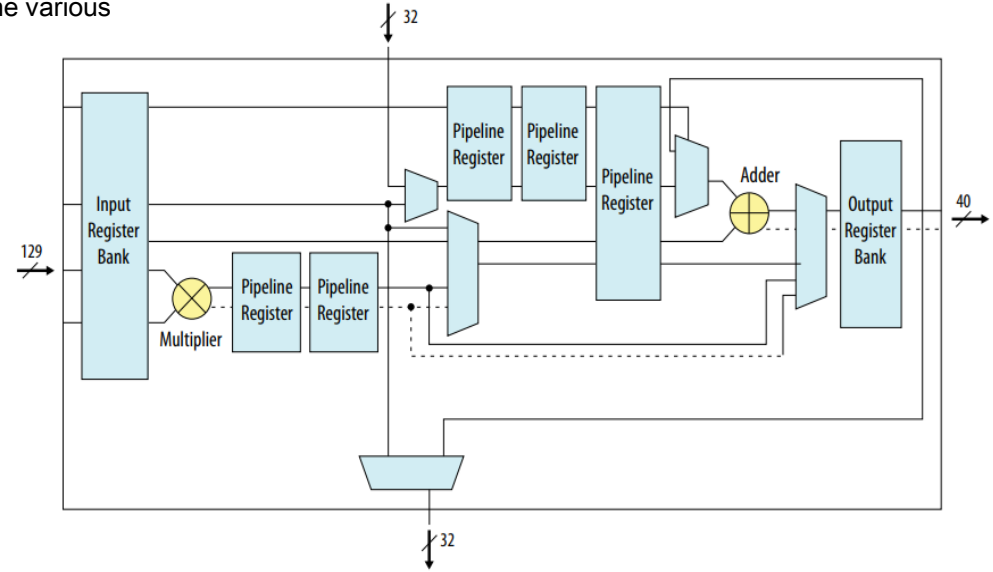
Unlike other interface standards, Intel® Ultra Path Interconnect (Intel® UPI) enables seamless access to data regardless of where it resides—core cache, FPGA cache, or memory. As a result, there's no need for redundant data storage and direct memory access transfers.

UPI is a low-latency coherent interconnect for scalable multiprocessor systems with a shared address space. It uses a directory-based home snoop coherency protocol with a transfer speed of up to 10.4 GT/s. Supporting processors typically have two or three UPI links.

source https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/item.html

Stratix® Series DSP Block

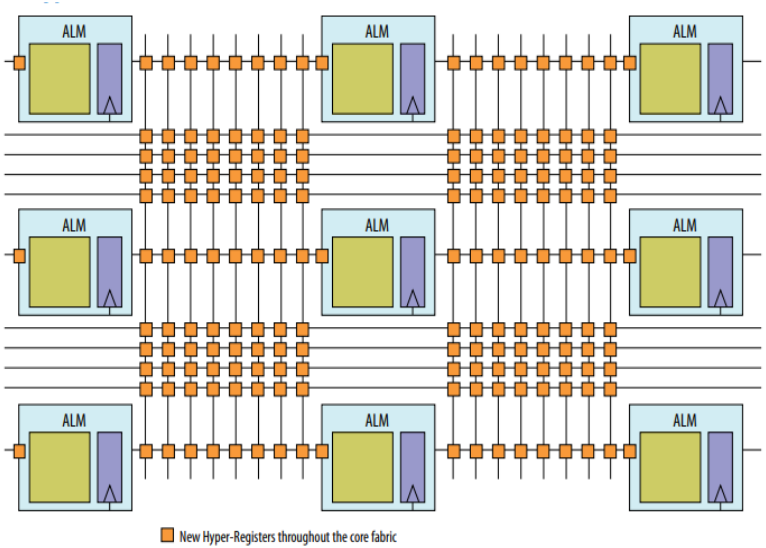
- DSP block is a power and area-efficient hardened IP block that balances compute resources with precision.
- Each DSP block can be independently configured or cascaded to scale for high-throughput processing.
- Block diagram shows the functional representation of the DSP block. The pipeline registers are embedded within the various circuits of the DSP block.



source https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/item.html

Intel® Hyperflex™ FPGA

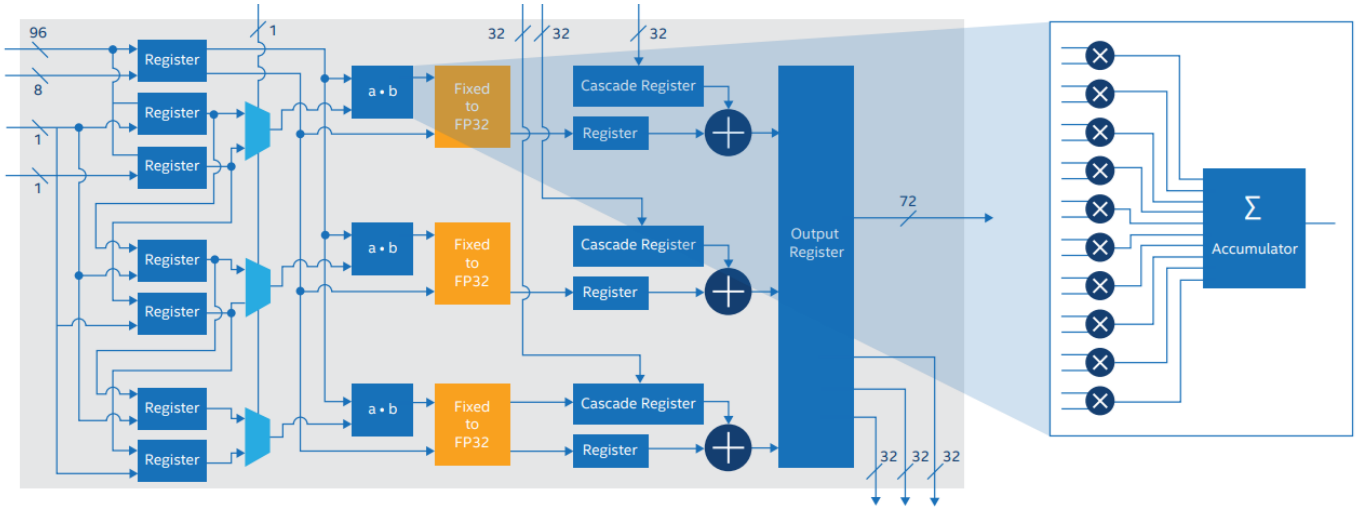
- The Hyper-Registers enable you to achieve core performance increases using key design techniques.
- If you implement these design techniques, the Hyper-Aware design tools automatically utilizes the Hyper-Registers to achieve maximum core clock frequency:
  - Fine grain Hyper-Retiming to eliminate critical paths
  - Zero-latency Hyper-Pipelining to eliminate routing delays
  - Flexible Hyper-Optimization for best-in-class performance



source https://www.intel.com/content/www/us/en/docs/programmable/683458/current/second-generation-core-architecture.html

Hardened AI Tensor Block

- The Intel Stratix 10 NX FPGA fabric includes new types of AI-optimized tensor arithmetic blocks called the AI Tensor Blocks.
- Each block contains three dot product units, each of which has ten multipliers and ten accumulators, for a total of 30 multipliers and 30 accumulators.
- The AI Tensor Block's architecture is tuned for common matrix-matrix or vector-matrix multiplications used in wide range of AI computations.



source https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/item.html

Intel® Stratix® Series Family

Intel® Stratix® 10 GX FPGA
- Designed to meet the high-performance demands of high-throughput systems.
- Launch date: **2013** (the largest, 10M - 2019)

Intel® Stratix® 10 SX SoC FPGA
- Features hard processor system with 64 bit quad-core ARM® Cortex-A53 processor.
- Launch date: **2013**

Intel® Stratix® 10 TX FPGA
- Delivers the most advanced transceiver capabilities in the industry by combining H- and E- transceiver tiles.
- Launch date: **2018**

Intel® Stratix® 10 MX FPGA
- Essential multi-function accelerator for high performance computing (HPC).
- Launch date: **2017**

Intel® Stratix® 10 DX FPGA
- Supports Ultra Path Interconnect for direct coherent connection to future select Xeon® Scalable processors.
- Launch date: **2019**

Intel® Stratix® 10 NX FPGA
- Designed to meet the high-performance demands of high-throughput systems.
- Launch date: **2020**

Intel® Stratix® 10 AX FPGA
- Delivers direct RF capabilities by integrating high-performance data converters.

source https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/item.html

Intel® Stratix® 10 GX/SX FPGA

Digital Logic Design with FPGA

PRODUCT LINE		GX 400 SX 400	GX 650 SX 650	GX 850 SX 850	GX 1100 SX 1100	GX 1650 SX 1650	GX 2100 SX 2100	GX 2500 SX 2500	GX 2800 SX 2800	GX 1660	GX 2110	GX 10M
Resources	Logic elements (LEs)[1]	378,000	612,000	841,000	1,325,000	1,624,000	2,005,000	2,422,000	2,753,000	1,679,000	2,073,000	10,200,000
	Adaptive logic modules (ALMs)	128,160	207,360	284,960	449,280	550,540	679,680	821,150	933,120	569,200	702,720	3,466,080
	ALM registers	512,640	829,440	1,139,840	1,797,120	2,202,160	2,718,720	3,284,600	3,732,480	2,276,800	2,810,880	13,864,320
	Hyper-Registers from Intel® Hyperflex™ FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric										
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees										
	M20K memory blocks	1,537	2,489	3,477	5,461	5,851	6,501	9,963	11,721	6,162	6,847	12,950
	M20K memory size (Mb)	30	49	68	107	114	127	195	229	120	134	253
	MLAB memory size (Mb)	2	3	4	7	8	11	13	15	9	11	55
	Variable-precision digital signal processing (DSP) blocks	648	1,152	2,016	2,592	3,145	3,744	5,011	5,760	3,326	3,960	3,456
	18 x 19 multipliers	1,296	2,304	4,032	5,184	6,290	7,488	10,022	11,520	6,652	7,920	6,912
	Peak fixed-point performance (TMACS)[2]	2.6	4.6	8.1	10.4	12.6	15.0	20.0	23.0	13.3	15.8	13.8
	Peak floating-point performance (TFLOPS)[3]	1.0	1.8	3.2	4.1	5.0	6.0	8.0	9.2	5.3	6.3	5.5
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection										–
	Hard processor system[4]	Quad-core 64-bit ARM* Cortex*-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 Cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4								–	–	–
		SX 400	SX 650	SX 850	SX 1100	SX 1650	SX 2100	SX 2500	SX 2800			
	Maximum user I/O pins	374	392	688	688	704	704	1160	1160	688	688	2,304
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	192	192	336	336	336	336	576	576	336	336	1152[5]
	Total full duplex transceiver count	24	24	48	48	96	96	96	96	48	48	48
	GXT full duplex transceiver count (up to 28.3 Gbps)	16	16	32	32	64	64	64	64	32	32	–
	GX full duplex transceiver count (up to 17.4 Gbps)	8	8	16	16	32	32	32	32	16	16	48
	PCI Express* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	1	1	2	2	4	4	4	4	2	2	4[6]

source https://www.intel.com/content/www/us/en/content-details/652478/intel-stratix-10-gx-fpga-and-intel-stratix-10-sx-soc-fpga-family-overview-product-table.html

Intel® Stratix® 10 TX FPGA

Digital Logic Design with FPGA

PRODUCT LINE		TX 400	TX 850	TX 850	TX 1100	TX 1100	TX 1650	TX 2100	TX 2500	TX 2500	TX 2800	TX 2800
Resources	Logic elements (LEs)[1]	378,000	841,000	841,000	1,325,000	1,325,000	1,679,000	2,073,000	2,422,000	2,422,000	2,753,000	2,753,000
	Adaptive logic modules (ALMs)	128,160	284,960	284,960	449,280	449,280	569,200	702,720	821,150	821,150	933,120	933,120
	ALM registers	512,640	1,139,840	1,139,840	1,797,120	1,797,120	2,276,800	2,810,880	3,284,600	3,284,600	3,732,480	3,732,480
	Hyper-Registers from Intel® Hyperflex™ FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric										
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees										
	eSRAM memory blocks	–	–	–	–	–	2	2	–	–	–	–
	eSRAM memory size (Mb)	–	–	–	–	–	94.5	94.5	–	–	–	–
	M20K memory blocks	1,537	3,477	3,477	5,461	5,461	6,162	6,847	9,963	9,963	11,721	11,721
	M20K memory size (Mb)	30	68	68	107	107	120	134	195	195	229	229
	MLAB memory size (Mb)	2	4	4	7	7	9	11	13	13	15	15
	Variable-precision digital signal processing (DSP) blocks	648	2,016	2,016	2,592	2,592	3,326	3,960	5,011	5,011	5,760	5,760
	18 x 19 multipliers	1,296	4,032	4,032	5,184	5,184	6,652	7,920	10,022	10,022	11,520	11,520
	Peak fixed-point performance (TMACS)[2]	2.6	8.1	8.1	10.4	10.4	13.3	15.8	20.0	20.0	23.0	23.0
	Peak floating-point performance (TFLOPS)[3]	1.0	3.2	3.2	4.1	4.1	5.3	6.3	8.0	8.0	9.2	9.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection										
	Hard processor system[4]	Quad-core 64-bit ARM* Cortex*-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 Cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4										
		Yes	Yes	Yes	Yes	Yes	–	–	Yes	Yes	Yes	Yes
	Maximum user I/O pins	384	440	440	440	440	440	440	440	296	440	296
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	192	216	216	216	216	216	216	216	144	216	144
	Total full duplex transceiver count	24	48	72	48	72	96	96	96	144	96	144
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or NRZ (up to 28.9 Gbps)	12 PAM-4 24 NRZ	12 PAM-4 24 NRZ	24 PAM-4 48 NRZ	12 PAM-4 24 NRZ	24 PAM-4 48 NRZ	36 PAM-4 72 NRZ	36 PAM-4 72 NRZ	36 PAM-4 72 NRZ	60 PAM-4 120 NRZ	36 PAM-4 72 NRZ	60 PAM-4 120 NRZ
	GXT transceiver count - NRZ (up to 28.3 Gbps)	0	16	16	16	16	16	16	16	16	16	16
	GX transceiver count - NRZ (up to 17.4 Gbps)	0	8	8	8	8	8	8	8	8	8	8
	PCI Express* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	0	1	1	1	1	1	1	1	1	1	1
	100G Ethernet MAC (no FEC) hard IP blocks	0	1	1	1	1	1	1	1	1	1	1
	100G Ethernet MAC + FEC hard IP blocks	4	4	8	4	8	12	12	12	20	12	20
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys										

source https://www.intel.com/content/www/us/en/content-details/652589/intel-stratix-10-tx-fpga-family-overview-product-table.html

Intel® Stratix® 10 MX FPGA

Digital Logic Design with FPGA

PRODUCT LINE		MX 1650	MX 1650	MX 1650	MX 2100	MX 2100	MX 2100	MX 2100
Resources	Logic elements (LEs)[1]	1,679,000	1,679,000	1,679,000	2,073,000	2,073,000	2,073,000	2,073,000
	Adaptive logic modules (ALMs)	569,200	569,200	569,200	702,720	702,720	702,720	702,720
	ALM registers	2,276,800	2,276,800	2,276,800	2,810,880	2,810,880	2,810,880	2,810,880
	Hyper-Registers from Intel® Hyperflex™ FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric						
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees						
	HBM2 high-bandwidth DRAM memory (GBytes)	8	16	8	8	8	16	8
	eSRAM memory blocks	2	2	2	2	2	2	2
	eSRAM memory size (Mb)	94.5	94.5	94.5	94.5	94.5	94.5	94.5
	M20K memory blocks	6,162	6,162	6,162	6,847	6,847	6,847	6,847
	M20K memory size (Mb)	120	120	120	134	134	134	134
	MLAB memory size (Mb)	9	9	9	11	11	11	11
	Variable-precision digital signal processing (DSP) blocks	3,326	3,326	3,326	3,960	3,960	3,960	3,960
	18 x 19 multipliers	6,652	6,652	6,652	7,920	7,920	7,920	7,920
	Peak fixed-point performance (TMACS)[2]	13.3	13.3	13.3	15.8	15.8	15.8	15.8
	Peak floating-point performance (TFLOPS)[3]	5.3	5.3	5.3	6.3	6.3	6.3	6.3
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection						
	Hard processor system[4]	–	–	–	–	–	–	–
	Maximum user I/O pins	656	656	584	640	656	656	584
	LVDS pairs 1.6 Gbps (RX or TX)	312	312	288	312	312	312	288
	Total full duplex transceiver count	96	96	96	48	96	96	96
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or NRZ (up to 28.9 Gbps)	0	0	36 PAM-4 72 NRZ	0	0	0	36 PAM-4 72 NRZ
	GXT transceiver count - NRZ (up to 28.3 Gbps)	64	64	16	32	64	64	16
	GX transceiver count - NRZ (up to 17.4 Gbps)	32	32	8	16	32	32	8
	PCI Express* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	4	4	1	2	4	4	1
	100G Ethernet MAC (no FEC) hard IP blocks	4	4	1	2	4	4	1
	100G Ethernet MAC + FEC hard IP blocks	0	0	12	0	0	0	12
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys						

source https://www.intel.com/content/www/us/en/content-details/652458/intel-stratix-10-mx-fpga-family-overview-product-table.html

Intel® Stratix® 10 DX FPGA

Digital Logic Design with FPGA

PRODUCT LINE		DX 1100	DX 2100	DX 2800
Resources	Logic elements (LEs)[1]	1,325,000	2,073,000	2,753,000
	Adaptive logic modules (ALMs)	449,280	702,720	933,120
	ALM registers	1,797,120	2,810,880	3,732,480
	Hyper-Registers from Intel® Hyperflex™ FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric		
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees		
	HBM2 High-bandwidth DRAM memory stacks	–	2	–
	HBM2 High-bandwidth DRAM memory size (GB)	–	8	–
	eSRAM memory blocks	–	2	–
	eSRAM memory size (Mb)	–	94.5	–
	M20K memory blocks	5,461	6,847	11,721
	M20K memory size (Mb)	107	134	229
	MLAB memory size (Mb)	7	11	15
	Variable-precision digital signal processing (DSP) blocks	2,592	3,960	5,760
	18 x 19 multipliers	5,184	7,920	11,520
	Peak fixed-point performance (TMACS)[2]	10.4	15.8	23.0
	Peak floating-point performance (TFLOPS)[3]	4.1	6.3	9.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection		
	Hard processor system[4]	Quad-core 64-bit Arm* Cortex*-A53 up to 1.5 GHz with 32KB I/D cache, NEON* coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4		
		Yes	–	–
	Maximum user I/O pins	528	612	816
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	264	306	408
	Total full duplex transceiver count - non return to zero (NRZ)	32	84	84
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or NRZ (up to 28.9 Gbps)	8 PAM-4, or 16 NRZ	12 PAM-4, or 24 NRZ	4 PAM-4, or 8 NRZ
	GXP transceiver count - NRZ (up to 16 Gbps)	16	60	76
	UPI/PCI Express* (PCIe*) Gen4 x16 hard intellectual property (IP) blocks (configurable for UPI or PCIe operation)	-	3	3
	PCI Express Gen4 x16 hard IP blocks (supports PCIe only)	1	-	1
	100G Ethernet media access control (MAC) + forward error correction (FEC) hard IP blocks	4	4	2
	Memory devices supported	Intel Optane™ Persistent Memory, DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3		

source https://www.intel.com/content/www/us/en/content-details/652414/intel-stratix-10-dx-fpga-family-overview-product-table.html

Intel® Stratix® 10 NX AI Optimized FPGA

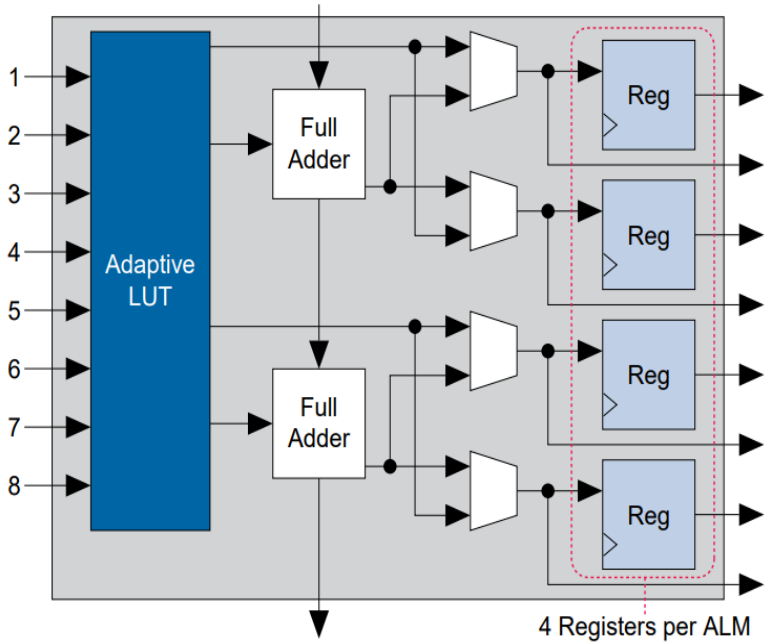
	PRODUCT LINE	NX 2100	NX 2100
Resources	Logic elements (LEs)[1]	2,073,000	2,073,000
	Adaptive logic modules (ALMs)	702,720	702,720
	ALM registers	2,810,880	2,810,880
	Hyper-Registers from Intel® Hyperflex™ FPGA Architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric	
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees	
	HBM2 high-bandwidth DRAM memory gigabytes (GB)	8	16
	eSRAM memory blocks	2	2
	eSRAM memory size (Mb)	94.5	94.5
	M20K memory blocks	6,847	6,847
	M20K memory size (Mb)	134	134
	MLAB memory size (Mb)	11	11
	AI Tensor Block	3,960	3,960
	Peak INT4 or BFP12 TOPS/TFLOPS[2]	286	286
	Peak INT8 or BFP16 TOPS/TFLOPS[2]	143	143
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection	
	Hard processor system[3]	–	–
	Maximum user I/O pins	656	584
	LVDS pairs 1.6 Gbps (RX or TX)	312	288
	Total full duplex transceiver count	96	96
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or non return to zero (NRZ) (up to 28.9 Gbps)	0	36 PAM-4 72 NRZ
	GXT transceiver count - NRZ (up to 28.3 Gbps)	64	16
	GX transceiver count - NRZ (up to 17.4 Gbps)	32	8
	PCI Expressa* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	4	1
	100G Ethernet MAC (no FEC) hard IP blocks	4	1
	100G Ethernet MAC + FEC hard IP blocks	0	12
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys	

source https://www.intel.com/content/www/us/en/content-details/626393/intel-stratix-10-nx-ai-optimized-fpga-product-table.html

Intel® Stratix® 10 ALM

Key features and capabilities of the ALM include:

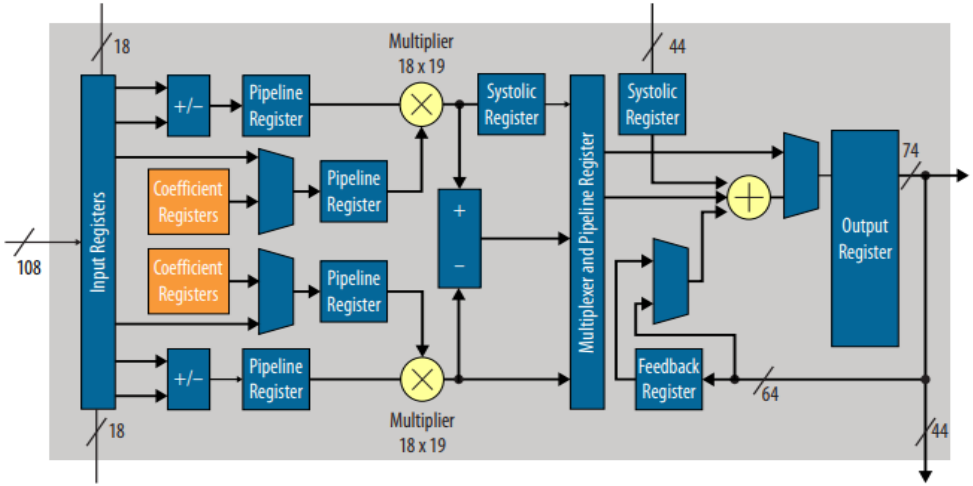
- High register count with 4 registers per 8-input fracturable LUT, operating in conjunction with the new Intel Hyperflex architecture, enables Intel Stratix 10 DX devices to maximize core performance at very high core logic utilization
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization



source https://www.intel.com/content/www/us/en/docs/programmable/683225/current/adaptive-logic-module-alm.html

Intel® Stratix® 10 DSP

- The Intel® Stratix® 10 DSP blocks are based upon the Variable Precision DSP Architecture used in Intel's previous generation devices. They feature hard fixed point and IEEE 754 compliant floating point capability.
- The DSP blocks can be configured to support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.



source https://www.intel.com/content/www/us/en/docs/programmable/683225/current/variable-precision-dsp-block.html

Intel® Stratix® 10 Applications

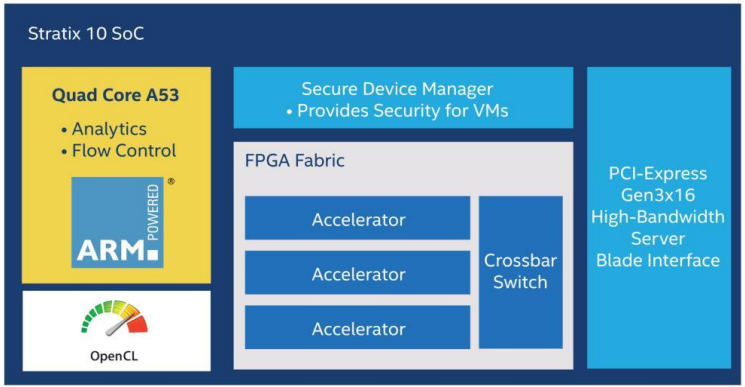
Digital Logic Design with FPGA

Unique to Intel® Stratix® 10 Devices:

- First FPGA devices to support Intel® Ultra Path Interconnect (UPI) for direct coherent connection to Intel® Xeon® Scalable processor.
- FPGA PCIe* hard IP with configuration up to Gen4 x16 at 16 Gbps.
- Intel® Hyperflex™ FPGA Architecture delivers up to 1 GHz performance, enabling breakthroughs in computational throughput.
- Hardened single-precision floating-point DSP block, compliant with IEEE 754 standard, delivers GPU-class floating performance at a fraction of the power.
- Hardened AI Tensor Block tuned for common matrix-matrix or vector-matrix multiplications in AI acceleration applications resulting in up to 143 INT8 TOPS or 286 INT4 TOPS.3
- Secure cloud solutions using the security features.

Can be used in:

- Data Center Acceleration
- Cognitive Computing
- Wireline
  - Bridging and Aggregation
  - Enabling New Network Infrastructure
- OTN/Data Center Interconnect
- Radars
- ASIC Prototyping and Emulation
- Cyber Security
  - Network Intrusion Detection and Prevention



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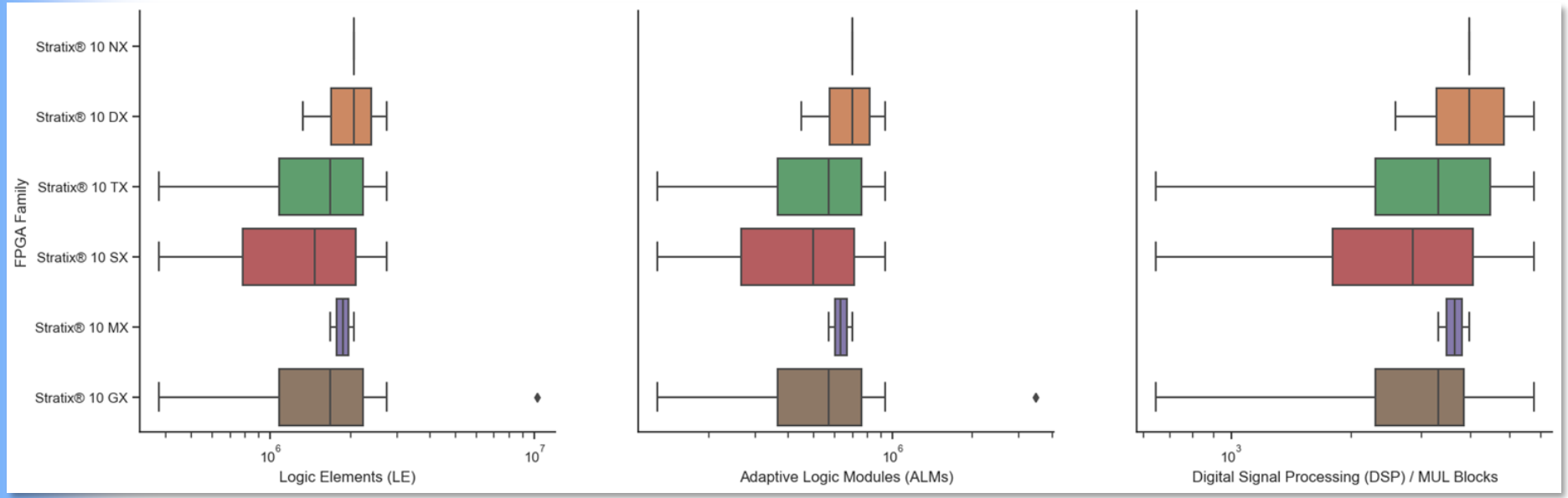
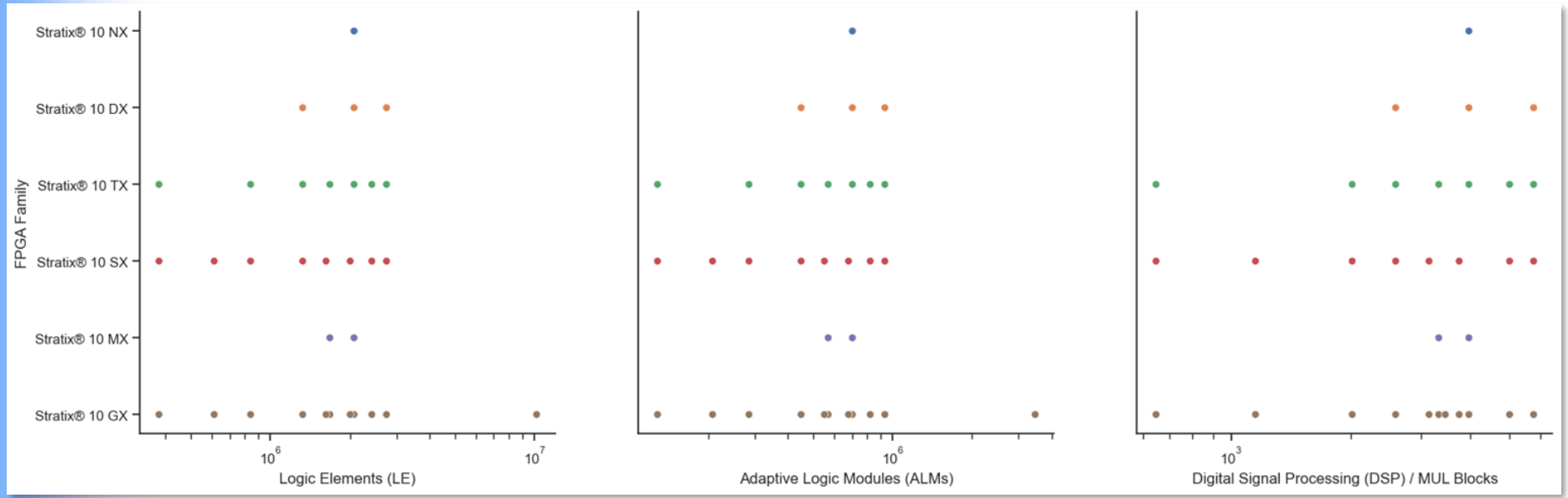
Intel® Stratix® Differences



Intel® Stratix® Differences



Intel Agilex® FPGA

	Intel Agilex® 9 FPGAs	Intel Agilex® 7 FPGAs	Intel Agilex® 5 FPGAs	Intel Agilex® 3 FPGAs
	Direct RF-Series	F-Series / I-Series / M-Series	E-Series / D-Series	
Logic Capacity Range (logic elements)	1.4M – 2.7M	573k – 4M	50k – 656k	Coming Soon
Memory (Max)	287 Mb	485 Mb (32 GB HBM2e option)	69 Mb	
DSP Type	Variable-Precision DSP Blocks	Variable-Precision DSP Blocks	Enhanced DSP with AI Tensor Blocks	
18x19 Multipliers (Max)	17,056	25,584	3,680	
Hard Processor Options	Quad-Core Arm Cortex-A53	Quad-Core Arm Cortex-A53	Dual-Core Arm Cortex-A76 Dual-Core Arm Cortex-A55	
High-Speed Interfaces (max data rate)	58 Gbps XCVRs 64 Gsps ADC/DAC	116 Gbps XCVRs	28 Gbps XCVRs	
Processor Interfaces	PCIe 4.0	PCIe 4.0/5.0, CXL	PCIe 4.0	
Memory Interfaces	DDR4, QDR IV	DDR4/5, LPDDR5, QDR IV	DDR4/5, LPDDR4/5, QDR IV	
I/O Count (Max)	660	768	444	
XCVR count (Max)	32	120	32	
Package Size (Min)	45x32mm	37.5x34mm	15x15mm	

Unprecedented Capabilities and Optimization for Target Applications

Higher Performance
More Features and Capabilities
Increasing Logic Capacity
Greater IO Bandwidth

Lower Power
More Cost Optimizations
Less Logic Capacity
Smaller Form Factors

source https://www.intel.com/content/www/us/en/products/details/fpga/agilex.html

Intel Agilex® FPGA

This series integrates industry leading wideband data converters with sample rates up to 64Gsps and medium-band data converters with hi-fidelity performance.

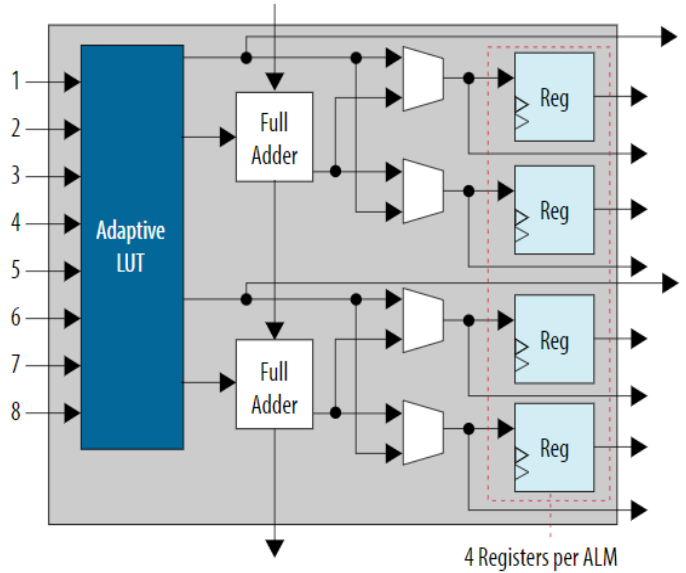
Midrange FPGAs optimized for applications requiring high performance, lower power, and smaller sizes.

Industry-leading fabric and IO speeds, ideal for the most bandwidth and compute-intensive applications.

Midrange FPGAs optimized for applications requiring high performance, lower power, and smaller sizes.

Intel® Agilex® ALM

- The Intel Agilex® FPGAs and SoCs use an enhanced adaptive logic module (ALM) similar to the previous generation Intel® FPGAs such as Intel® Arria® 10 and Intel® Stratix® 10 FPGAs.
- The enhanced ALM allows for efficient implementation of logic functions and easy IP conversion between Intel Agilex® 5 FPGAs and Intel® Arria® 10 and Intel® Stratix® 10 FPGAs.



source https://www.intel.com/content/www/us/en/docs/programmable/683213/current/arithmetic-mode.html

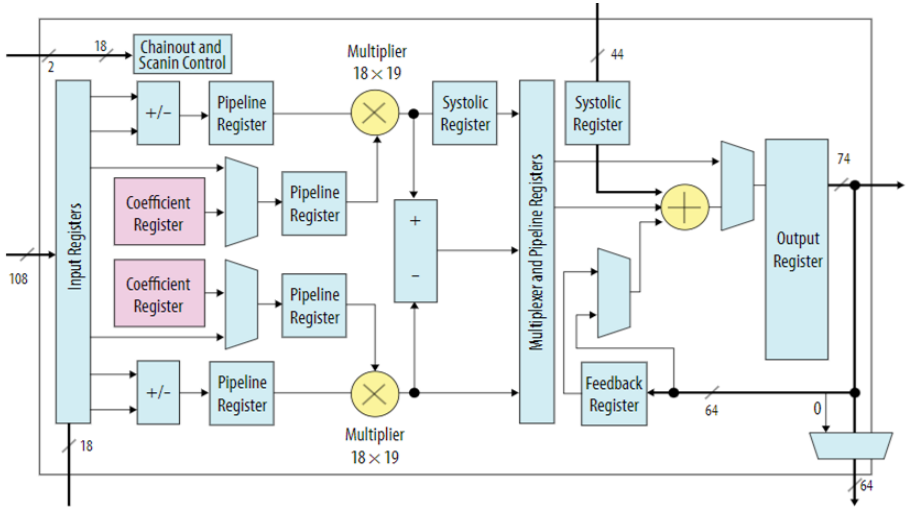
Intel® Agilex® DSP

The Intel Agilex® 7 FPGAs and SoCs carry over the variable-precision DSP architecture from previous Intel® FPGAs with hard fixed point and IEEE 754-compliant floating point capabilities.
In fixed point mode, you can configure the DSP blocks to support signal processing with precisions from 9×9 up to 54×54:

- Increased 9×9 multipliers count, with three 9×9 multipliers for every 18×19 multiplier
- A pipeline register increases the maximum DSP block operating frequency and reduces the power consumption
- Dynamically switch multiplier inputs through scanin and chainout signals
- Compile each DSP block independently as four 9×9, two 18×19, or one 27×27 multiply-accumulate

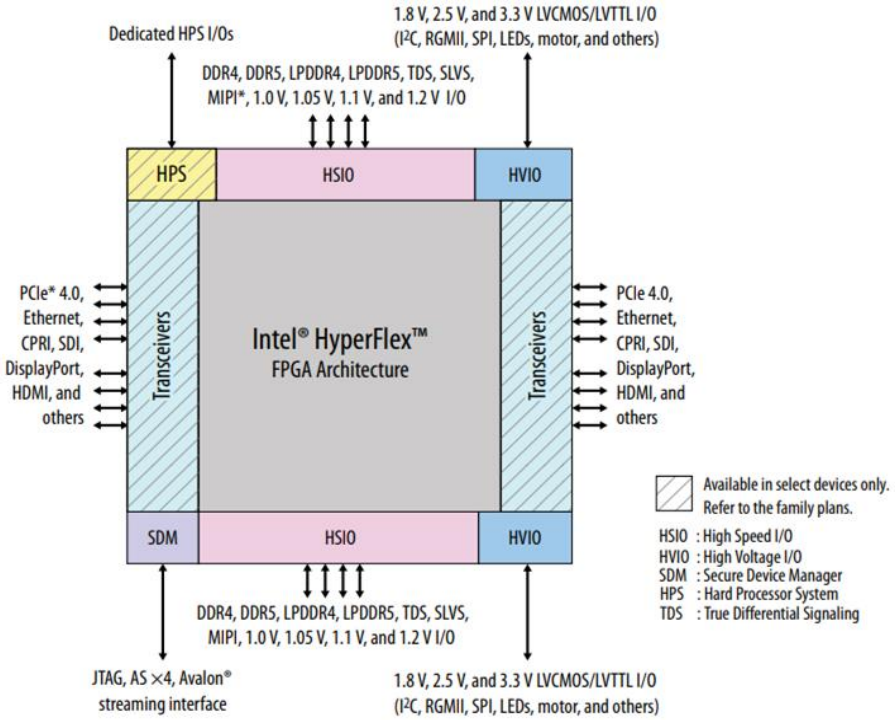
The variable-precision DSP supports floating point addition, multiplication, multiply-add, and multiply-accumulate:

- Single-precision 32-bit arithmetic FP32 floating point mode
- Half-precision 16-bit arithmetic FP16 and FP19 floating point modes, and BFLOAT16 floating point format
- With a dedicated 64-bit cascade bus, you can cascade multiple variable-precision DSP blocks to efficiently implement even higher-precision DSP functions.



source https://www.intel.com/content/www/us/en/docs/programmable/683458/current/variable-precision-dsp-in-fpgas-and-socs.html

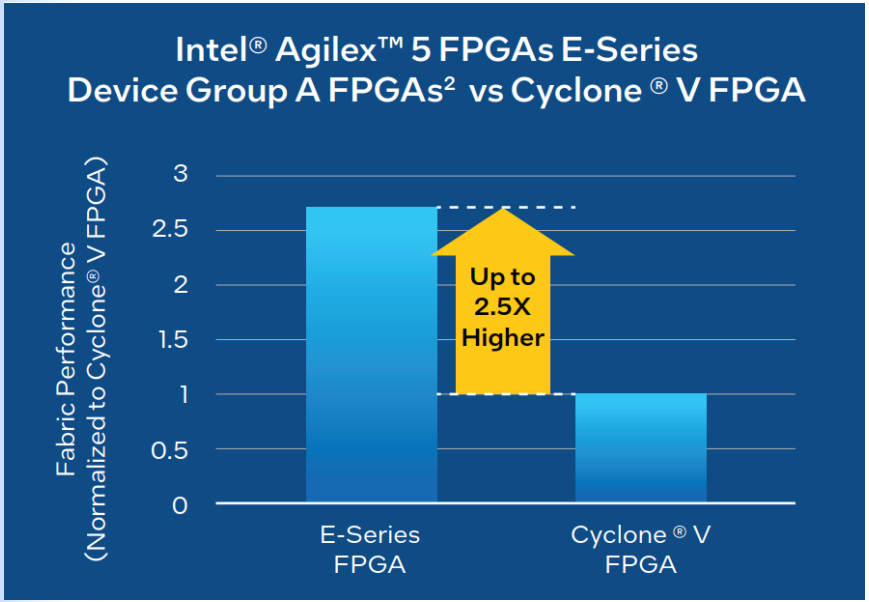
Intel Agilex 5 FPGAs and SoCs

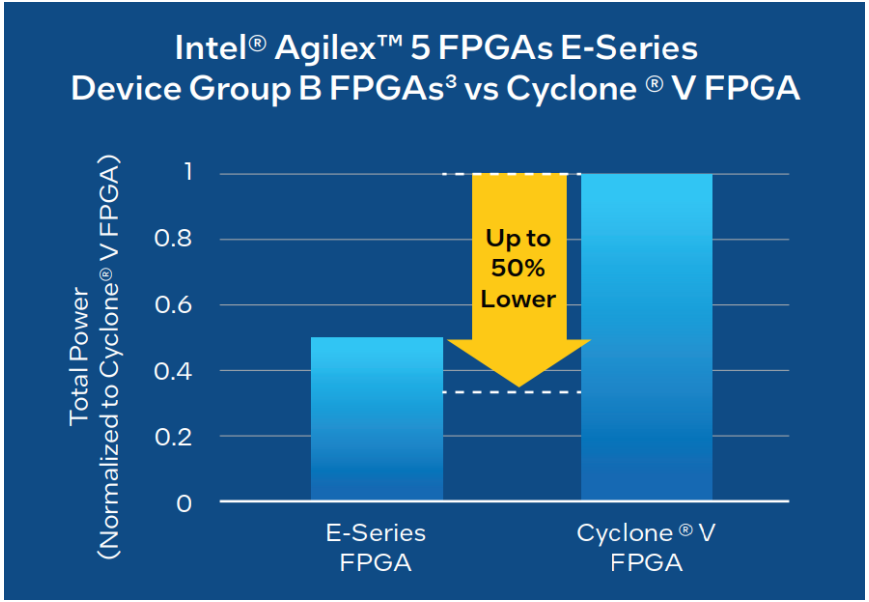


source https://www.intel.com/content/www/us/en/docs/programmable/683458/current/fpgas-and-socs-block-diagram.htm

https://www.intel.com/content/www/us/en/docs/programmable/762191/current/fpgas-and-socs-block-diagram.html

Intel® Agilex 5 FPGA





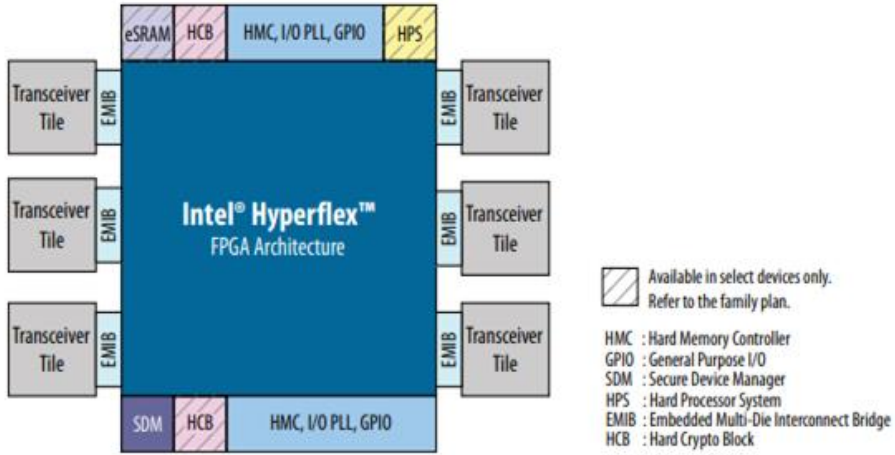
2) Device Group A FPGAs is at 0.8 V when compared with Cyclone V FPGA.

3) Device Group B FPGAs is at 0.75 V, 100% fabric utilization, and 350 MHz when compared with Cyclone V FPGA.

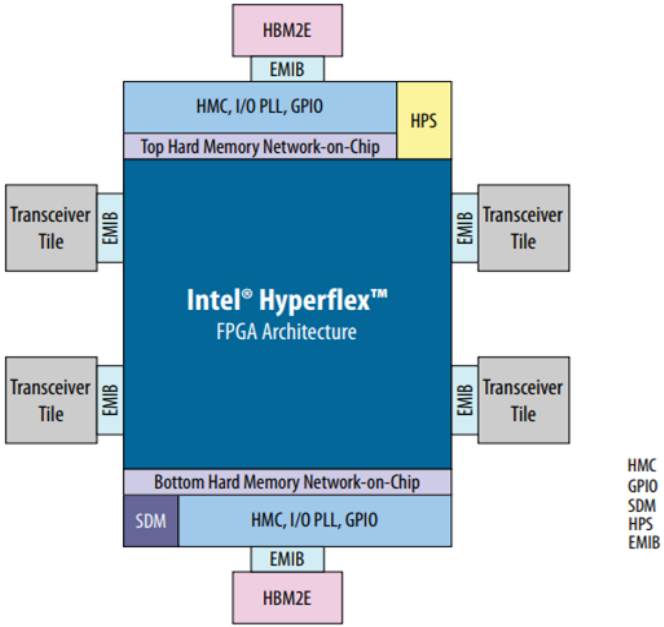
Intel Agilex 7 FPGAs and SoCs

Digital Logic Design with FPGA

Intel Agilex 7 FPGAs and SoCs F-Series and I-Series Block Diagram



Intel Agilex 7 FPGAs and SoCs M-Series Block Diagram



source https://www.intel.com/content/www/us/en/docs/programmable/683458/current/fpgas-and-socs-block-diagram.htm

https://www.intel.com/content/www/us/en/docs/programmable/762191/current/fpgas-and-socs-block-diagram.html

Intel® Agilex® Applications

Network/Communications

- Networking applications such as Next-Gen Firewall (NGFW) require highperformance data paths, deep memory buffers, and high-bandwidth connectivity. These physical requirements combined with increased software processing functions have pushed non-FPGA based deployments past their functional limits.

Broadcast

- Applications such as high-end 8K cameras add further complexity, with metadata added to each pixel for high-definition rate (HDR), sensor data, and color correction to name a few.
- Transferring the massive image sensor pipeline to the processing device requires high bandwidth connectivity using protocols such as 100G Ethernet, 12G Serial Digital Interface (SDI), PCIe, DisplayPort or HDMI, as does displaying or storing the processed data.

Cloud

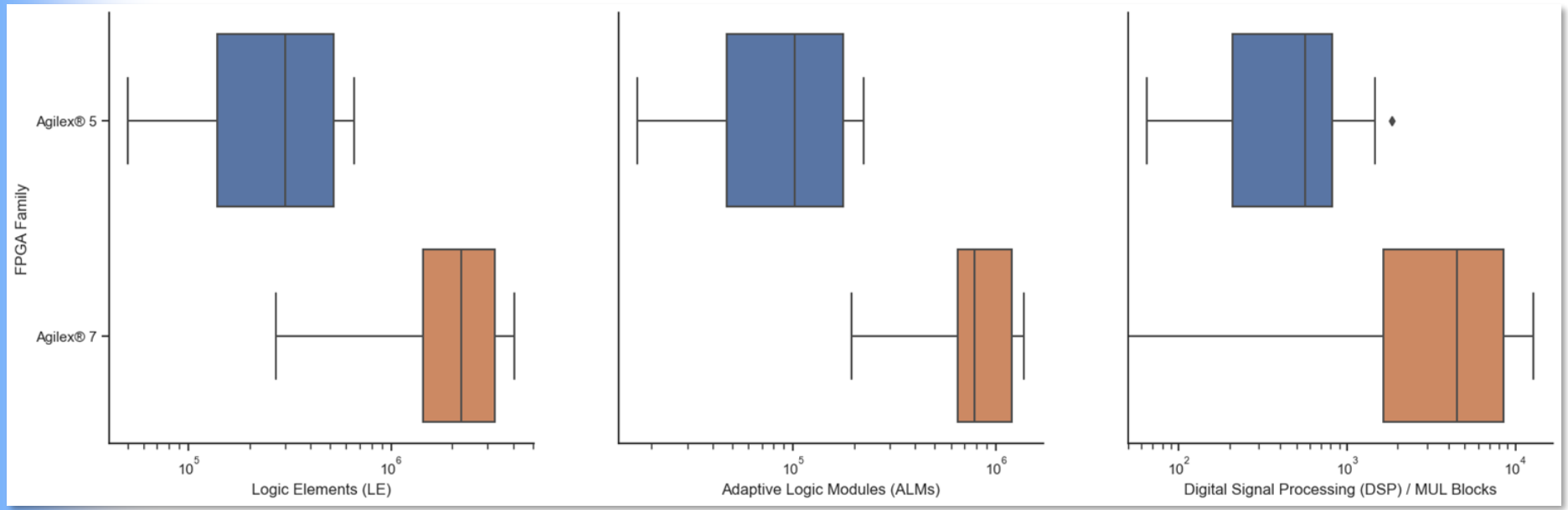
- High-memory bandwidth is a requirement for common artificial intelligence (AI), network processing, data analytics, and cryptocurrency mining applications.
- In cryptocurrency mining, the costs associated with electricity and removing waste heat can be significant. High powerefficiency directly translates to profitability.

Test and Measurement

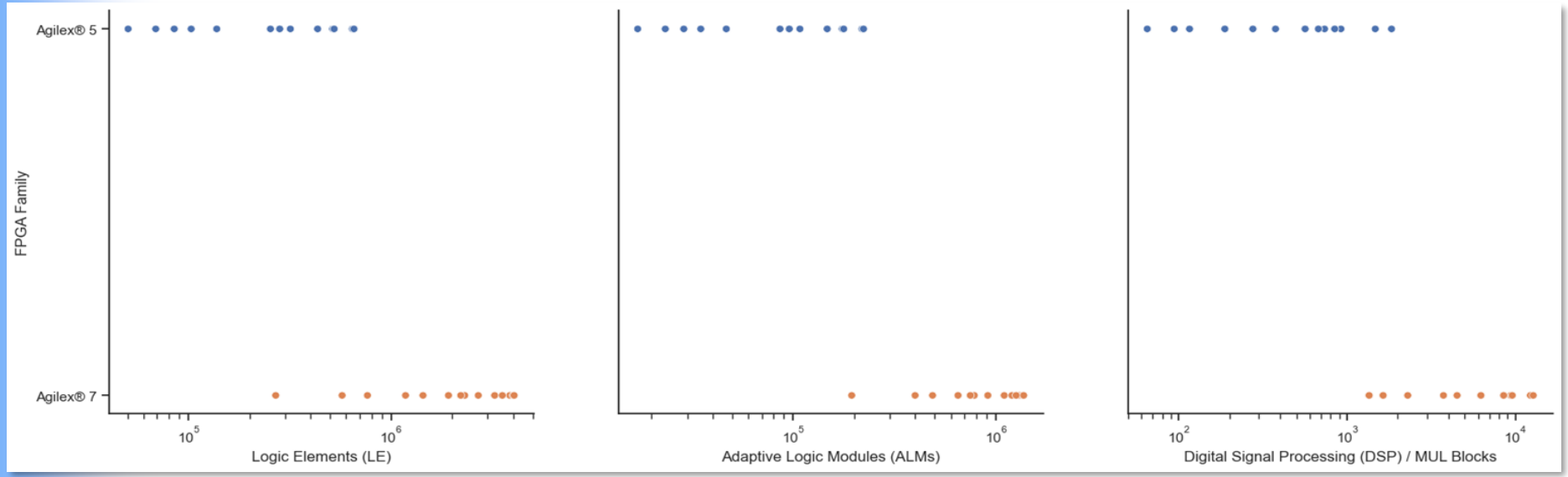
- Ethernet speeds are growing exponentially, spiking the need for ethernet testing. As 400GbE is still rolling out, 800GbE is already under development. Customers are demanding testers capable of supporting a variety of speeds and protocols.

source https://www.intel.com/content/www/us/en/products/docs/programmable/agilex-7-fpga-m-series-memory-bandwidth-sb.html

Intel® Agilex® Differences



Intel® Agilex® Differences

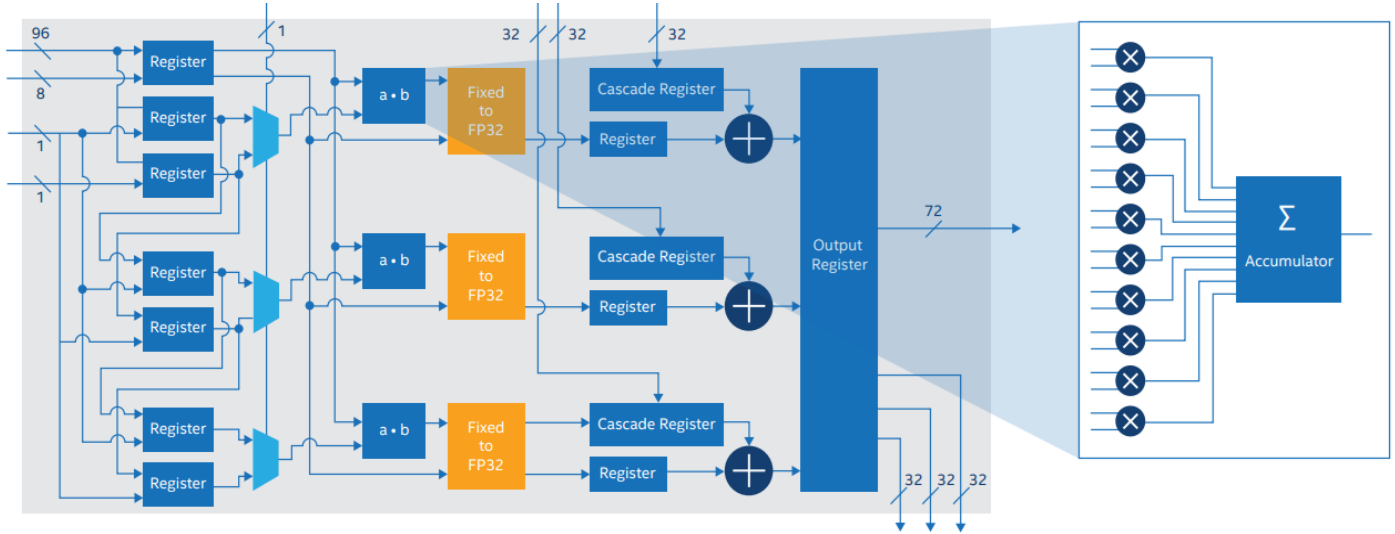


Digital Logic
Design with FPGA

Intel FPGA and AI

Hardened AI Tensor Block

- The Intel Stratix 10 NX FPGA fabric includes new types of AI-optimized tensor arithmetic blocks called the AI Tensor Blocks.
- Each block contains three dot product units, each of which has ten multipliers and ten accumulators, for a total of 30 multipliers and 30 accumulators.
- The AI Tensor Block's architecture is tuned for common matrix-matrix or vector-matrix multiplications used in wide range of AI computations.



source https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/item.html

Intel® Stratix® 10 NX AI Optimized FPGA

Digital Logic Design with FPGA

PRODUCT LINE		NX 2100	NX 2100
Resources	Logic elements (LEs)[1]	2,073,000	2,073,000
	Adaptive logic modules (ALMs)	702,720	702,720
	ALM registers	2,810,880	2,810,880
	Hyper-Registers from Intel® Hyperflex™ FPGA Architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric	
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees	
	HBM2 high-bandwidth DRAM memory gigabytes (GB)	8	16
	eSRAM memory blocks	2	2
	eSRAM memory size (Mb)	94.5	94.5
	M20K memory blocks	6,847	6,847
	M20K memory size (Mb)	134	134
	MLAB memory size (Mb)	11	11
	AI Tensor Block	3,960	3,960
	Peak INT4 or BFP12 TOPS/TFLOPS[2]	286	286
	Peak INT8 or BFP16 TOPS/TFLOPS[2]	143	143
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection	
	Hard processor system[3]	–	–
	Maximum user I/O pins	656	584
	LVDS pairs 1.6 Gbps (RX or TX)	312	288
	Total full duplex transceiver count	96	96
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or non return to zero (NRZ) (up to 28.9 Gbps)	0	36 PAM-4 72 NRZ
	GXT transceiver count - NRZ (up to 28.3 Gbps)	64	16
	GX transceiver count - NRZ (up to 17.4 Gbps)	32	8
	PCI Expressa* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	4	1
	100G Ethernet MAC (no FEC) hard IP blocks	4	1
	100G Ethernet MAC + FEC hard IP blocks	0	12
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys	

source https://www.intel.com/content/www/us/en/content-details/626393/intel-stratix-10-nx-ai-optimized-fpga-product-table.html

Intel® Agilex 5 Tensor Block

The DSP blocks incorporated into the programmable-logic fabric of Intel Agilex 5 inherit the design of the variable precision DSP blocks in the Intel® Agilex 7 family.

The DSP blocks in Intel Agilex 5 devices add features derived from the tensor block used in Stratix® 10 NX.

These blocks have been completely redesigned to provide a 5X performance boost while maintaining the same die size area compared to the prior generation of DSP blocks, thereby significantly increasing the performance-per-watt metric.

Applications	Multiplier	Capabilities per DSP Block		Improvement*
		Earlier Intel Agilex Devices	Enhanced DSP with AI Tensor Block*	
AI, Signal Processing	INT8	4 OPS	20 OPS	5X
	INT9	4 Multipliers	6 Multipliers	50%
Signal Processing	16-bit Complex Multiplier	Needs 2 DSP Blocks	1 DSP Block	2X

*Available in Intel® Agilex 5 FPGAs D-Series and Intel® Agilex 5 FPGAs E-Series.

source https://www.intel.com/content/www/us/en/products/details/fpga/agilex/5/e-series.html

Intel FPGA AI

Intel FPGAs enable real-time, low-latency, and low-power deep learning inference combined with the following advantages:

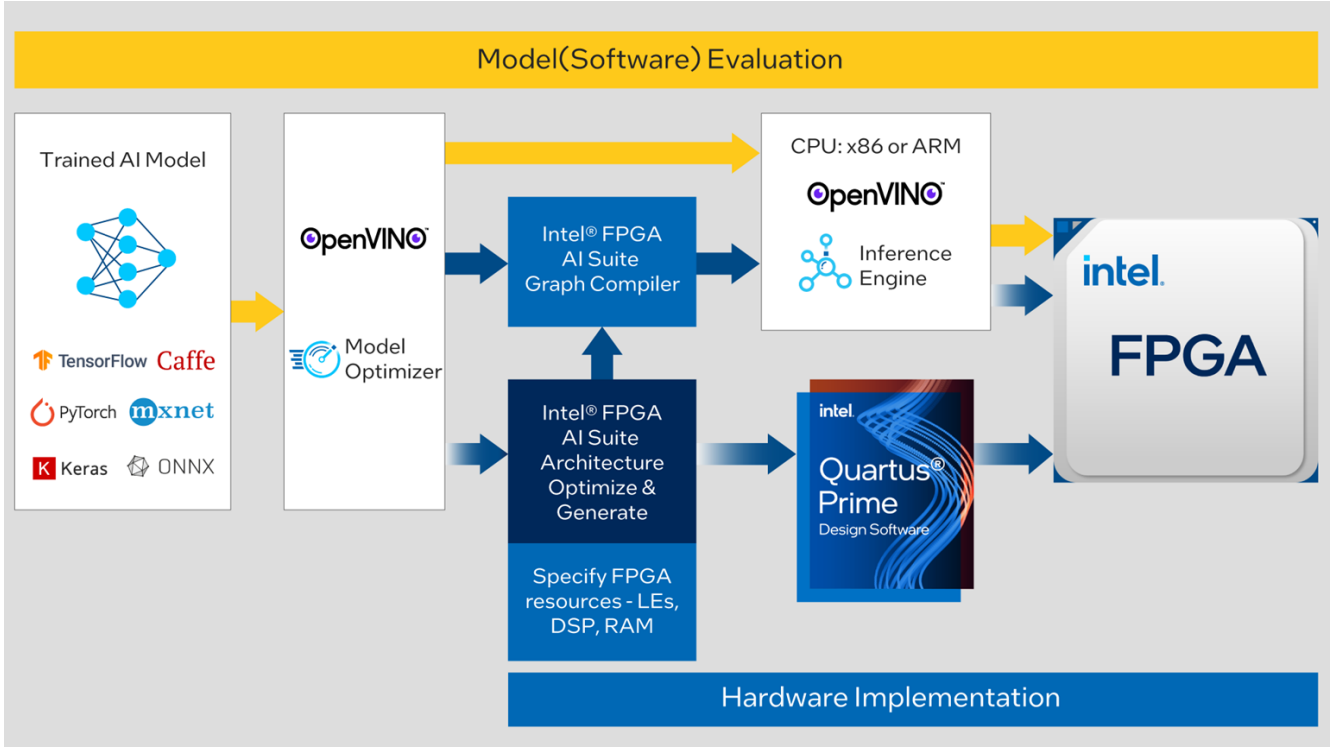
- I/O flexibility
- Reconfiguration
- Ease of integration into custom platforms
- Long lifetime

Key Features:

- High Performance e.g. 3,679 Resnet-50 frames per second at 90% FPGA utilization on Intel Agilex® 7 FPGA M-Series.
- Supports integration with custom IP such as ADCs/DACs, video, and Ethernet to achieve the smallest footprint and lowest latency.
- AI Front End Support such as TensorFlow, Caffe, Pytorch, MXNet, Keras, and ONNX.

source https://www.intel.com/content/www/us/en/software/programmable/fpga-ai-suite/overview.html

FPGA AI Inference Development Flow

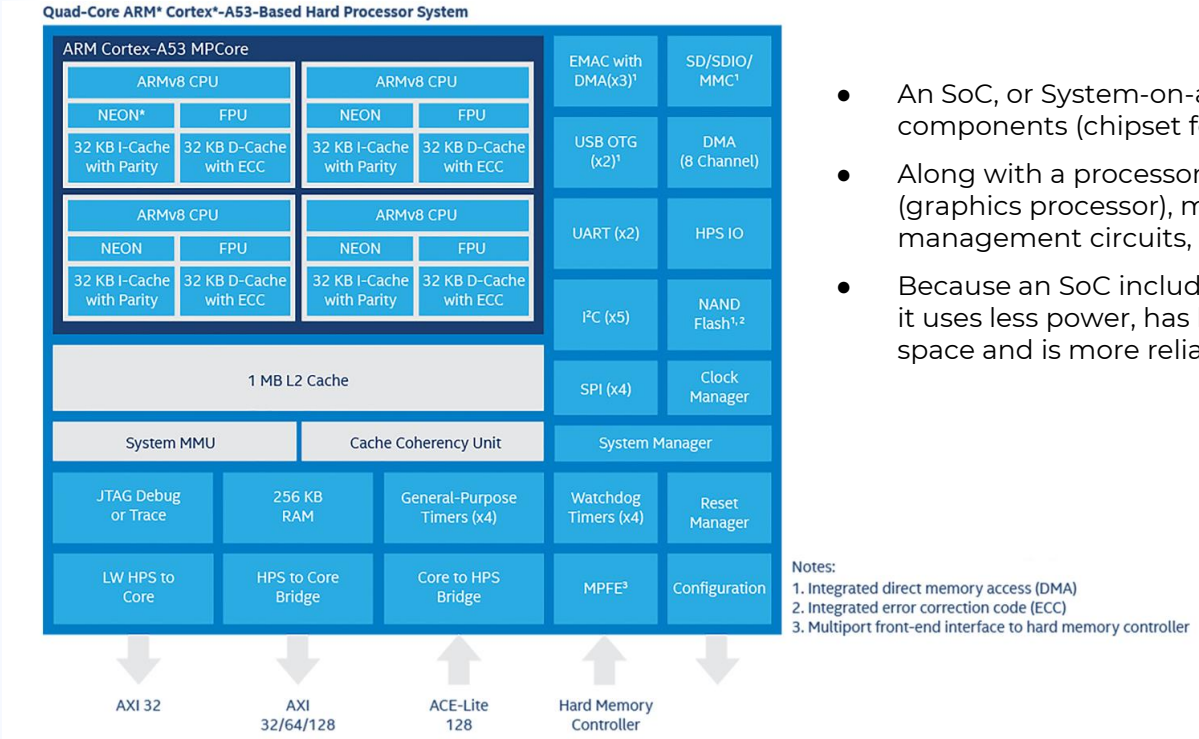


source https://www.intel.com/content/www/us/en/software/programmable/fpga-ai-suite/overview.html

Digital Logic
Design with FPGA

System on Programmable Chip

System-on-a-Chip



- An SoC, or System-on-a-Chip, integrates almost all of these components (chipset features) into a single silicon chip.
- Along with a processor, the SoC usually contains a GPU (graphics processor), memory, USB controller, power management circuits, and wireless radios.
- Because an SoC includes both the hardware and software, it uses less power, has better performance, requires less space and is more reliable than multichip systems.

source https://www.intel.com/content/www/us/en/support/articles/000056236/intel-nuc.html
https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/article.html

Intel Products with HPS

There are several families of Intel® SoC devices:

- Altera® Cyclone® V SoC
- Altera Arria® V SoC
- Intel Arria 10 SoC
- Intel Stratix® 10 SoC

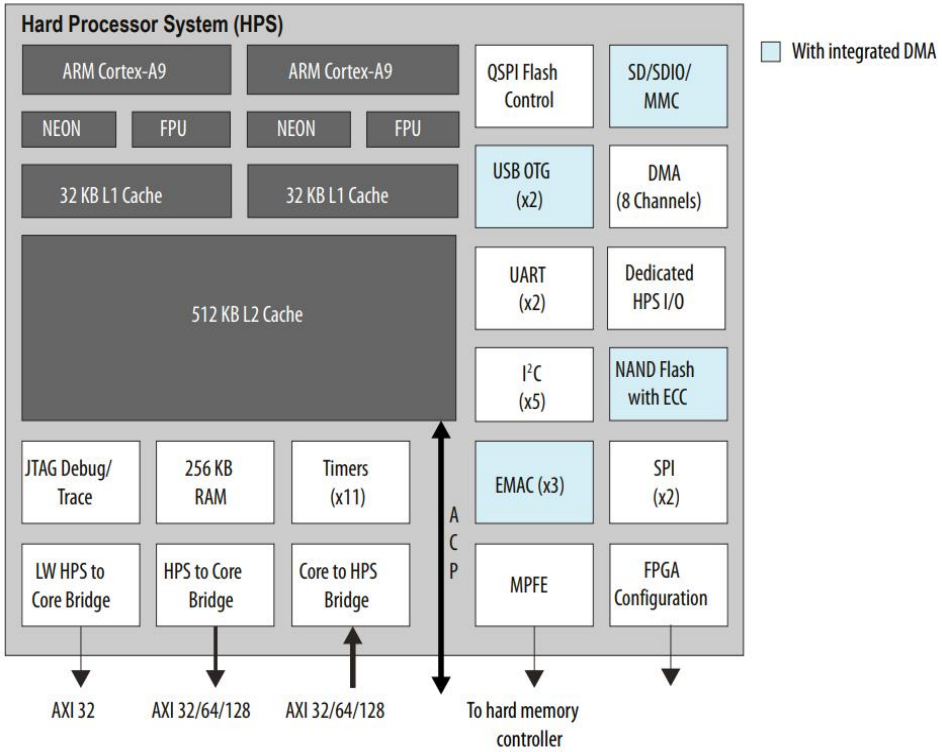
HPS Module	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Microprocessor Unit Subsystem (MPU)	Single / Dual Cortex®-A9	Dual Cortex-A9	Dual Cortex-A9	Quad Cortex-A53
Cache Coherency Controller	Accelerator coherency port (ACP)	ACP	ACP	Cache Coherency Unit (CCU)
System Memory Management Unit	No	No	No	Yes
On-Chip RAM	64 KB	64 KB	256 KB	256 KB
Error Correction Code (ECC) Controller	No	No	Yes	Yes

source https://www.intel.com/content/www/us/en/docs/programmable/683648/current/differences-among-intel-soc-device-families.html

SoC with Hard Processor System

Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates



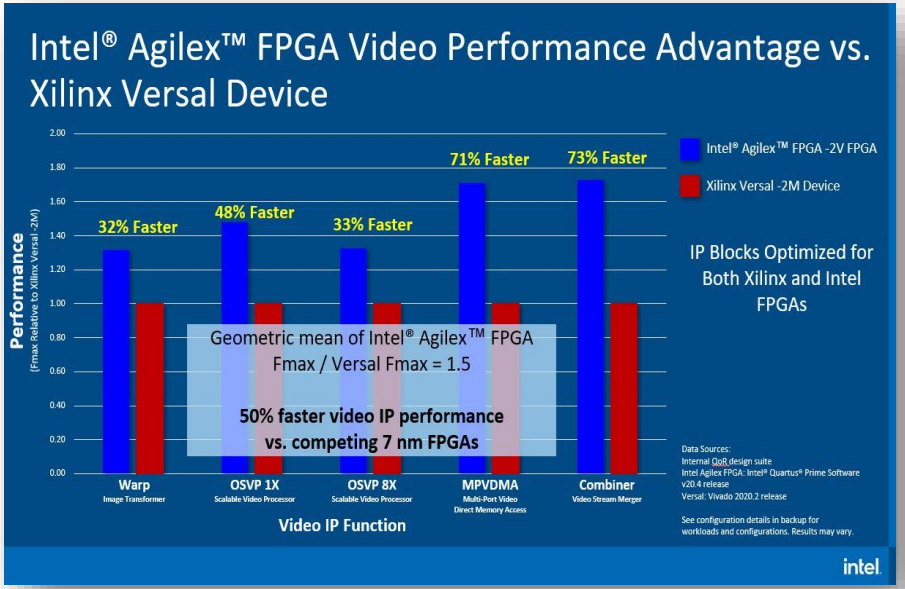
source https://www.intel.com/content/www/us/en/docs/programmable/683332/current/soc-with-hard-processor-system.html

Digital Logic
Design with FPGA

Battle for FPGA Leadership

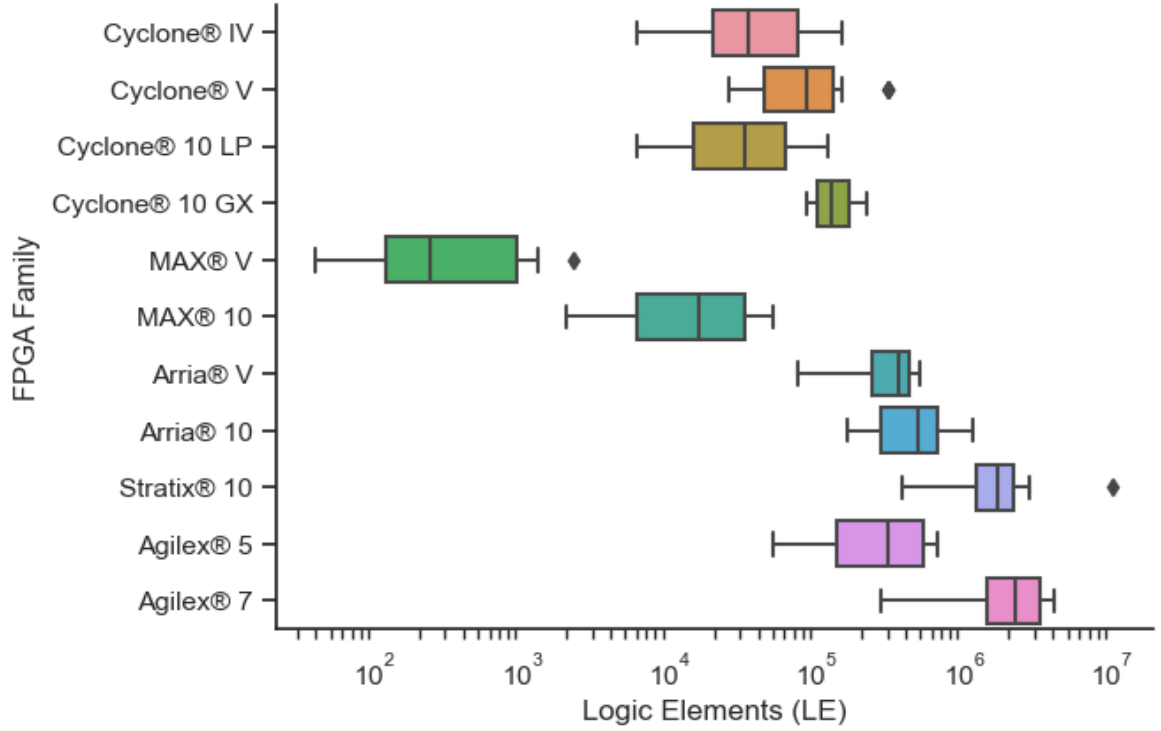
AMD vs. Intel: Battle For FPGA Leadership

- Given AMD's Xilinx acquisition, questions arise about who will hold FPGA leadership going forward.
- Intel Agilex FPGA achieves 30-50% higher performance and 2x performance per watt than Xilinx Versal.
- Intel further leads in innovation due to leadership transceivers, chiplet and 3D packaging, and AI performance.
- October 2020 AMD Completes Acquisition of Xilinx for approximately $135 billion.
- December 2015 Intel Completes Acquisition of Altera for 16,7 billion USD.

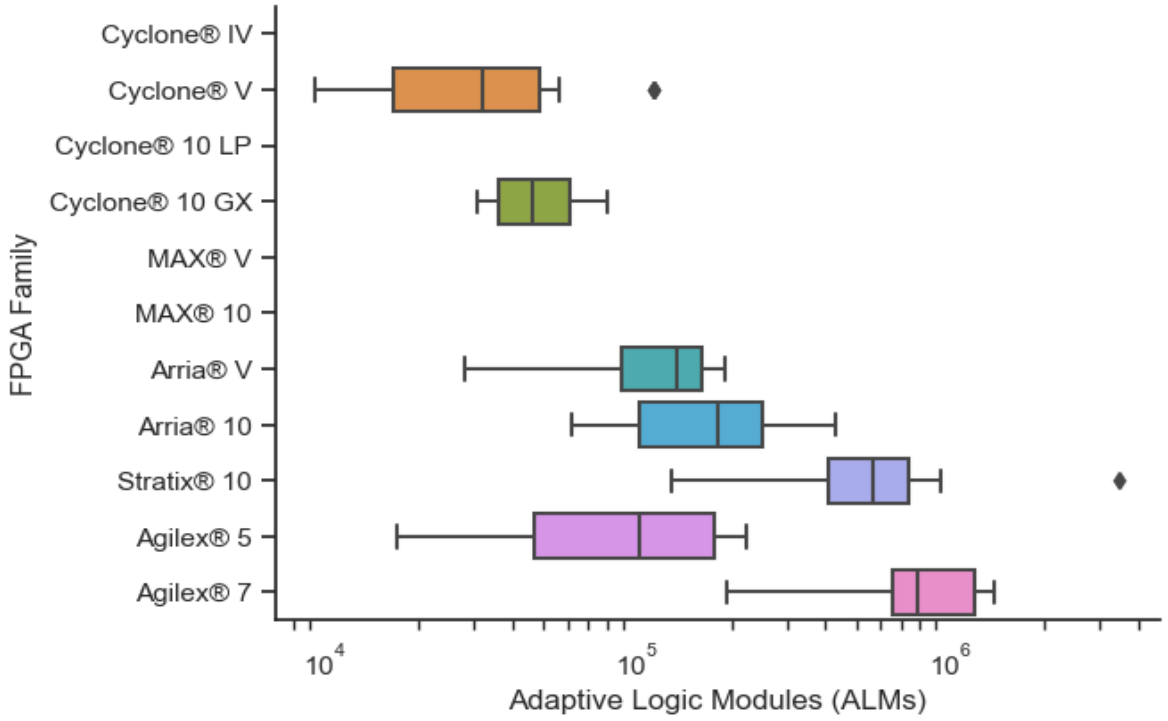


source https://seekingalpha.com/article/4473345-amd-vs-intel-battle-for-fpga-leadership

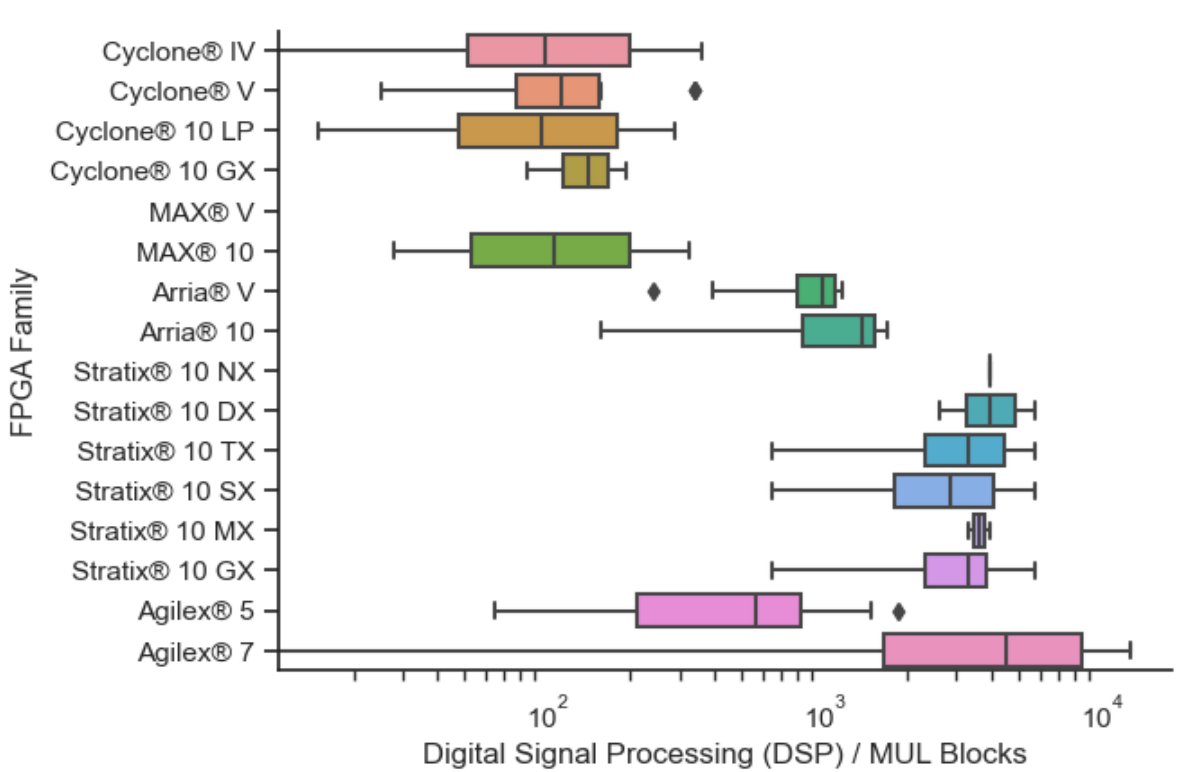
Logic Elements Comparison



ALM Comparison



DSP Comparison



FPGA families with MUL blocks:

- MAX 10
- Cyclone IV