Digital Logic
Design with FPGA

Design Flow with Quartus

Configuration

Outline

- In-System programming
- JTAG
- Non-volatile FPGAs
  - User Flash Memory
  - Configuration Flash Memory
- Quartus Prime Programmer

FPGA Programming

- FPGA programming information must be stored somewhere to program device at power on
- Use external EEPROM, CPLD, or CPU to program
- Two programming methods
  - Active: FPGA controls programming sequence automatically at power on
  - Passive: Intelligent host (typically CPU) controls programming
- Also programmable through JTAG connection

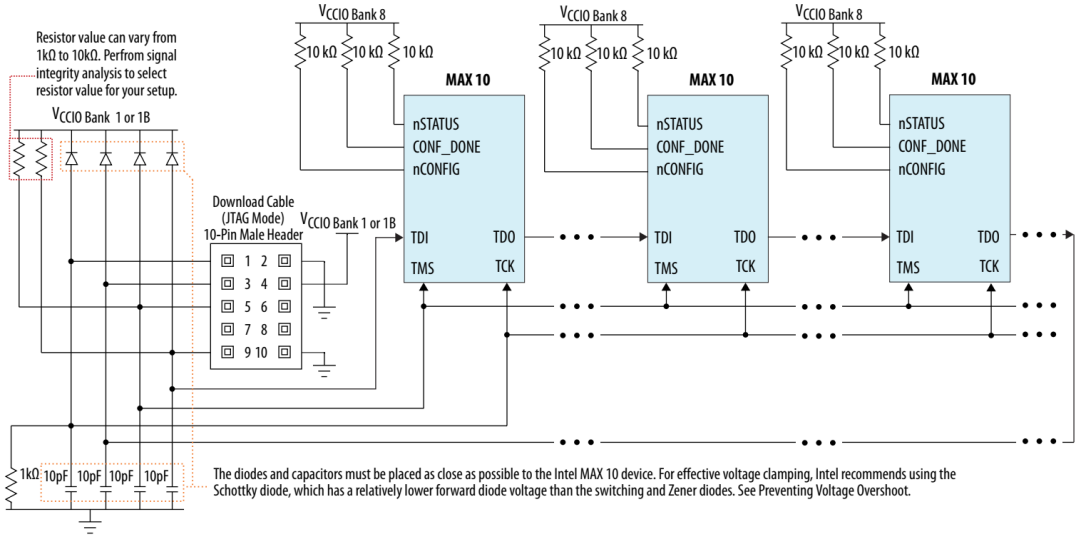
Configuration scheme	Name	Interface	External memory/ configuration device	Width of data	Configuration time
active	AS	serial	EPCS/EPCQ device	1 or 4	moderate
passive	PS	serial	MAX CPLD or uP with flash	1	moderate
		serial	download cable	1	moderate
	FPP	parallel	MAX CPLD or uP with flash	8, 16, 32	fast
	JTAG	serial	download cable	1	slow
	CvP	serial	external PCIe host	1, 2, 4, 8	fastest

source: Intel® MAX® 10 FPGA Configuration User Guide, https://www.intel.com/content/www/us/en/docs/programmable/683865/current/fpga-configuration-overview.html

In-System Programming

JTAG

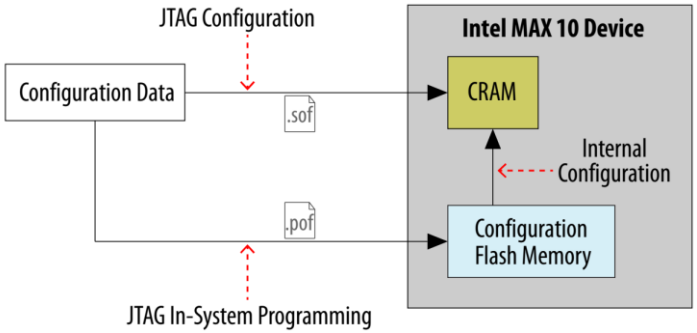
- Established by the Joint Test Action Group (commonly used name for IEEE Std. 1149.1)
- Developed to provide a simple method, called boundary scan, for testing devices
- Used as a convenient way of configuring programmable devices in-system
- TDI (Test Data In), TDO (Test Data Out), TMS (Test Mode Select), TCK (Test Clock)



Setup for JTAG Multi-Device Configuration

source: Intel® MAX® 10 FPGA Configuration User Guide, https://www.intel.com/content/www/us/en/docs/programmable/683865/current/fpga-configuration-overview.html

In-System Programming



JTAG Configuration and Internal Configuration for Intel MAX 10 Devices

.sof (SRAM Object File)

Used to configure FPGAs directly from Quartus Prime through download cable

Always generated by default during a full compilation by the Assembler

.pof (Programming Object File)

Used to program CPLDs and configuration devices

.jam/.jbc

ASCII file used by processors and test equipment to program devices via JTAG

source: Intel® MAX® 10 FPGA Configuration User Guide, https://www.intel.com/content/www/us/en/docs/programmable/683865/current/fpga-configuration-overview.html

Non-Volatile FPGAs

- MAX II, MAX V, and MAX10 families
- Full-featured FPGA capabilities plus
  - User Flash Memory (UFM)
  - Configuration Flash Memory (CFM)
- Instant on
- Low-cost

Features	Capacity
Endurance	Counts to at least 10,000 program/erase cycles
Data retention (after 10,000 program/erase cycles)	20 years at 85 ºC 10 years at 100 ºC
Maximum operating frequency	Serial interface 10M02, 10M04, 10M08, 10M16, 10M25: 7.25 MHz 10M40, 10M50: 4.81 MHz Parallel interface 10M02: 7.25 MHz 10M02, 10M04, 10M08, 10M16, 10M25, 10M40, 10M50: 16.00 MHz
Data length	Stores data of up to 32 bits length in parallel

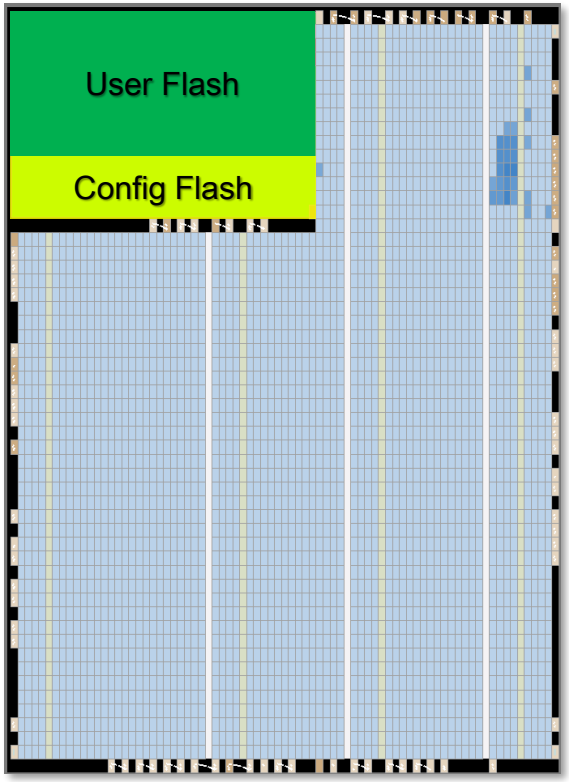
source https://www.intel.com/content/www/us/en/docs/programmable/683180/18-0/user-flash-memory-overview.html

Non-Volatile FPGAs

- Two internal flash regions
  - Configuration Flash Memory (CFM)
    Single or dual image
    Compressed or uncompressed image
  - User Flash Memory (UFM)
    Code space
    RAM initialization
    Data storage
    General scratch page

Device	Page Size (Kb)	Pages / Sector	# of Sectors	Total UFM Size (Kb)
10M02	16	3	2	96
10M04	16	8	1	128
10M08	16	8	2	256
10M16	32	4	2	256
10M25	32	4	2	256
10M40	64	4	2	512
10M50	64	4	2	512

Internal Flash memory



source: https://www.intel.com/content/www/us/en/docs/programmable/683180/18-0/user-flash-memory-overview.html

Non-Volatile FPGAs

In certain configuration modes, CFM can be used as UFM

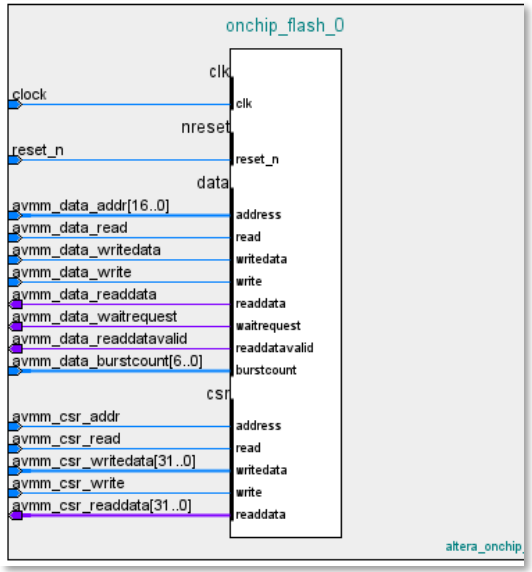
- Using CFM sectors as UFM

Supported Configuration Modes (1)	CFM2	CFM1	CFM0
Single uncompressed image with RAM preload	Uncompressed Image (w/RAM preload)		
Single compressed image with RAM preload	Compressed Image (w/RAM preload)		
Dual Boot	Compressed Image 2		Compressed Image 1
Single uncompressed image without RAM preload	UFM	Uncompressed Image	
Single compressed image without RAM preload	UFM		Compressed Image

Note 1: Except for 10M02 devices

- User Flash Memory Block
  - Used only through an Avalon Memory Maped slave interface using On-Chip Flash IP core
  - Combination of soft and hard IPs

On-Chip Flash Intel FPGA IP

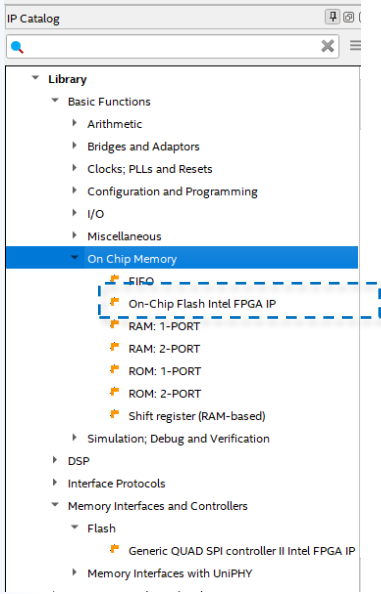


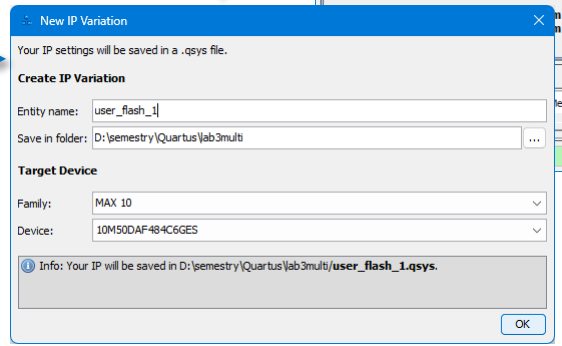
source: https://www.intel.com/content/www/us/en/docs/programmable/683180/18-0/user-flash-memory-overview.html

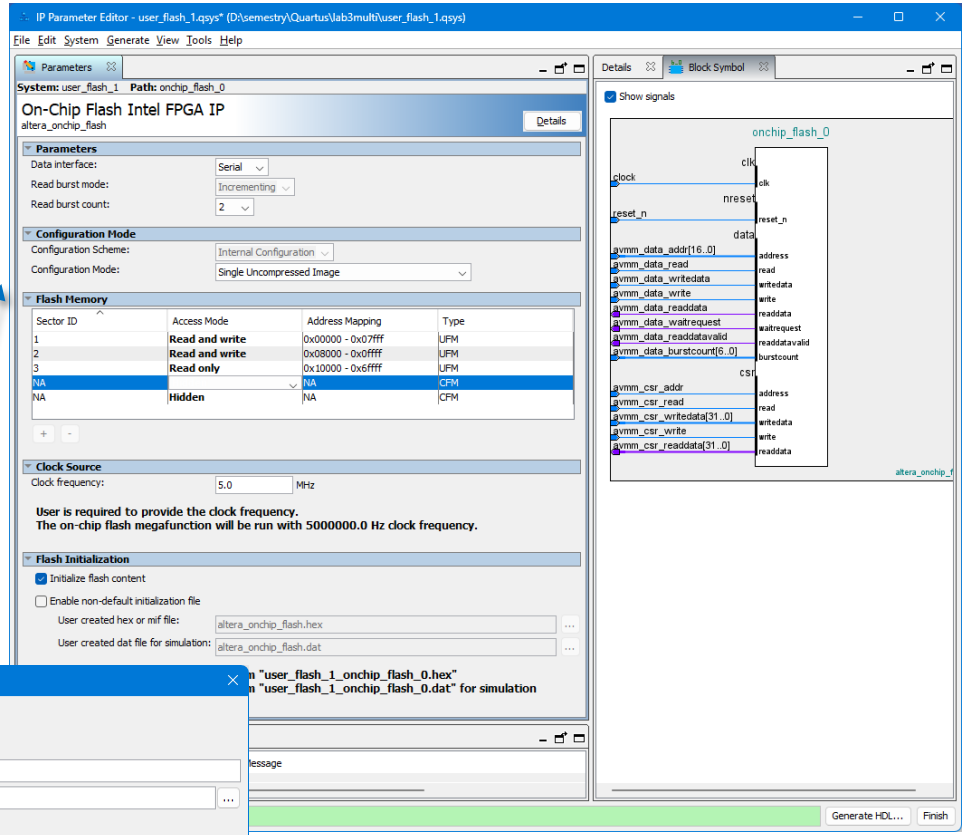
Non-Volatile FPGAs

On-chip flash usage scenario:

- Choose the On-Chip Flash IP from Quartus IP Catalog
- Parametrize using IP parameter editor
- Generate HDL code
- Instantiate in user HDL
- Avalon rules must be manually followed







Specify custom IP name and the session will be saved as <*ip name*>.**qsys**

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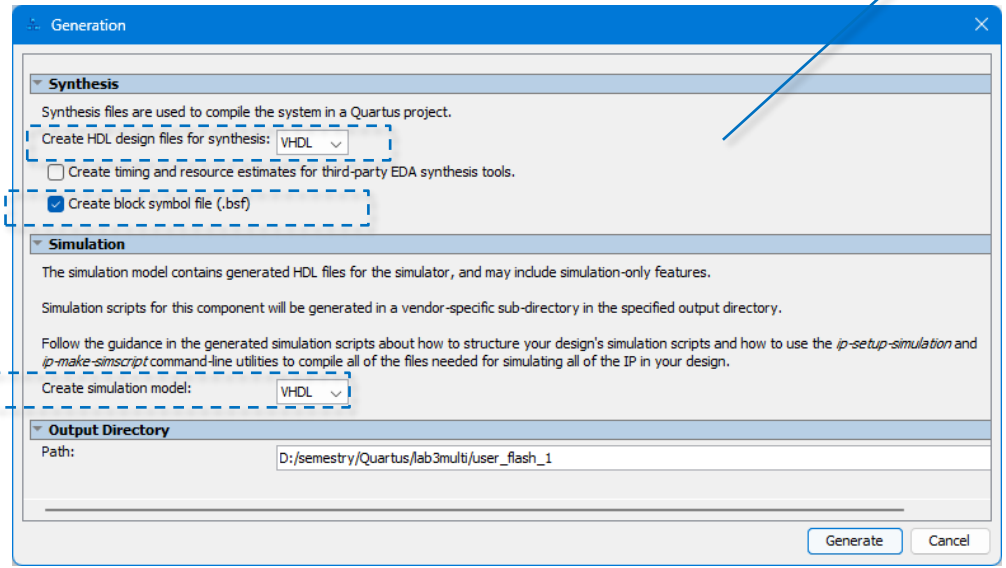
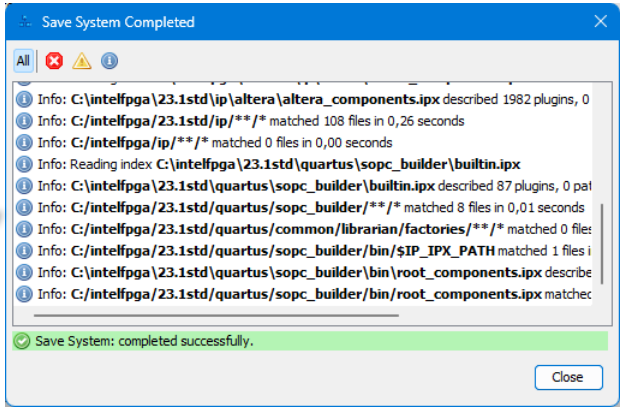




Parameter editor will add **.qsys** file to the current project

Digital Logic Design with FPGA

source: https://www.intel.com/content/www/us/en/docs/programmable/683180/18-0/user-flash-memory-overview.html

Quartus Prime Programmer

- By default, the Compiler's Assembler module generates the primary device programming files at the end of full compilation
- You can start the Assembler independently any time after design place and route to generate primary device programming files:

  .sof (SRAM Object File)

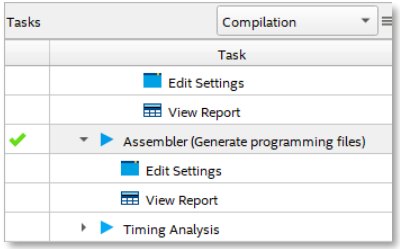
  Used to configure FPGAs directly from Quartus Prime through download cable

  .pof (Programming Object File)

  A binary file that contains the data for programming non-volatile MAX® 10, MAX® V, MAX® II, or flash memory devices that can configure Intel FPGA devices

  .jam/.jbc

  ASCII file used by processors and test equipment to program devices via JTAG

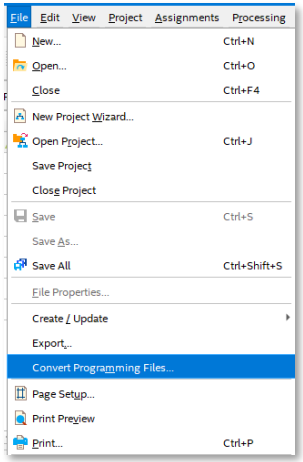


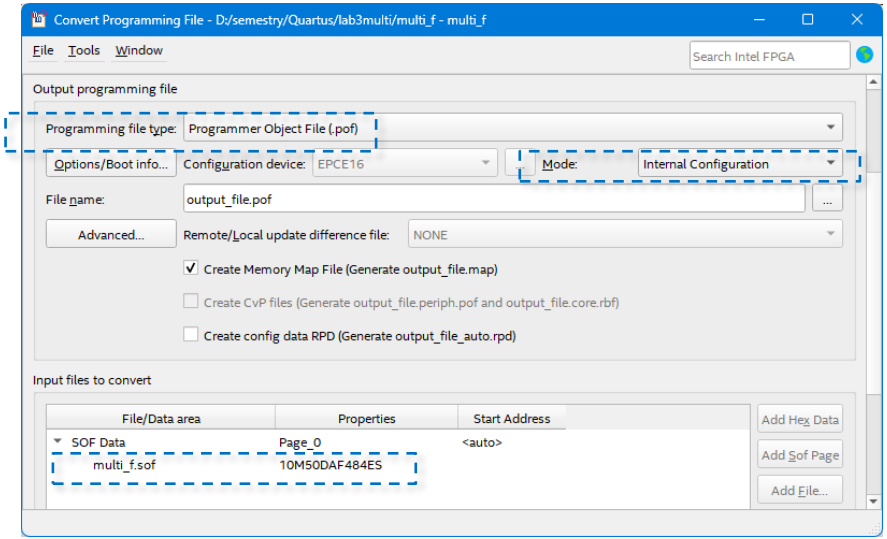

```
Tcl: quartus_asm --read_settings_files=on --write_settings_files=off multi_f -c multi_f
```


source: Intel® MAX® 10 FPGA Configuration User Guide, https://www.intel.com/content/www/us/en/docs/programmable/683865/current/fpga-configuration-overview.html

Quartus Prime Programmer

- Convert programming files GUI



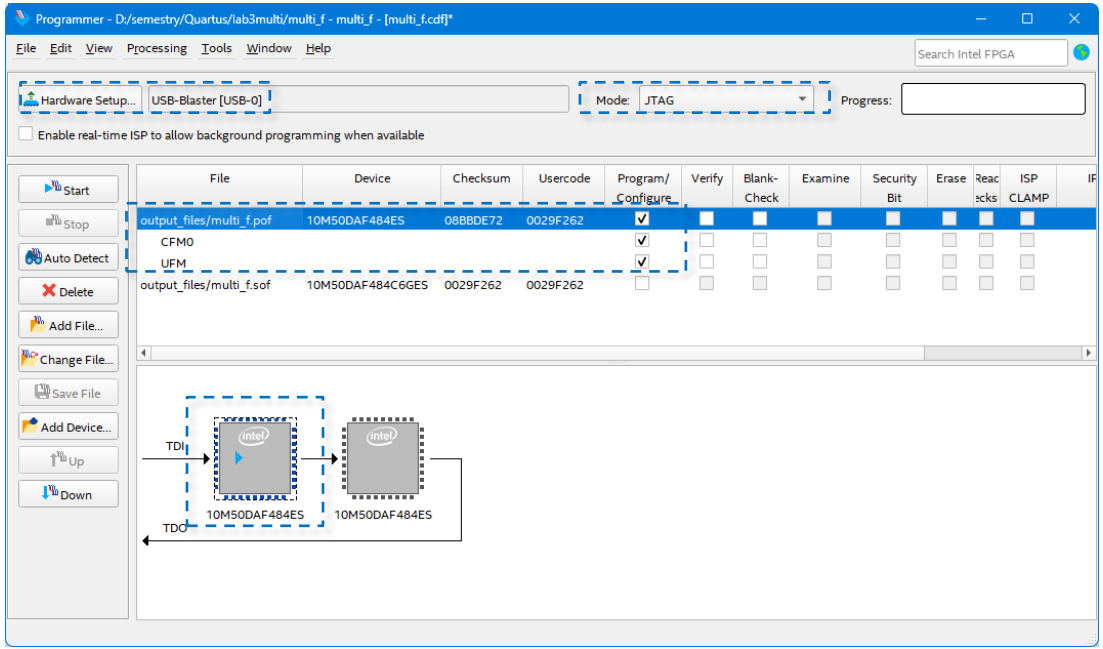


- Internal Configuration
  - Uses a .pof file for internal configuration of the MAX 10 device's Configuration Flash Memory (CFM) and User Flash Memory (UFM) via a download cable Quartus Prime Programmer

source: Intel® MAX® 10 FPGA Configuration User Guide, https://www.intel.com/content/www/us/en/docs/programmable/683865/current/fpga-configuration-overview.html

Quartus Prime Programmer

- Programmer allows you to program and configure Intel® CPLD, FPGA, and configuration devices
- Prior to programming or configuration:
  - Generate and specify the primary programming files
  - Setup the programming hardware
  - Set the configuration mode in the Programmer



source: https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-software/fpga-development-tools-support.html