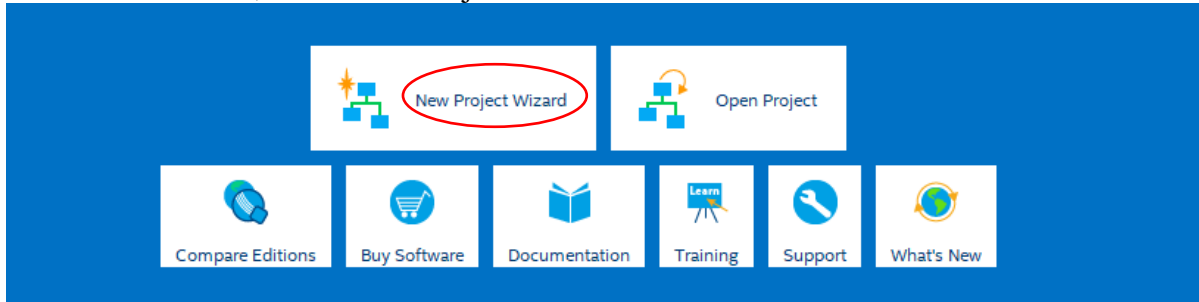


## Quartus Prime – quick start

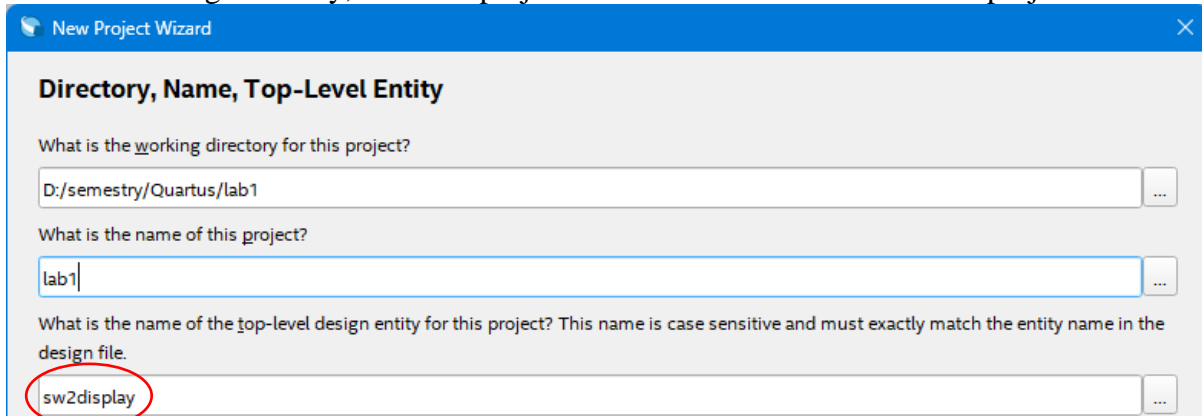
### 1. Preparing the project

Launch Quartus Prime

In the start window, select New Project Wizard



Select a working directory, enter the project name and the name of the main project unit



**New Project Wizard**

**Directory, Name, Top-Level Entity**

What is the working directory for this project?

D:/semester/Quartus/lab1

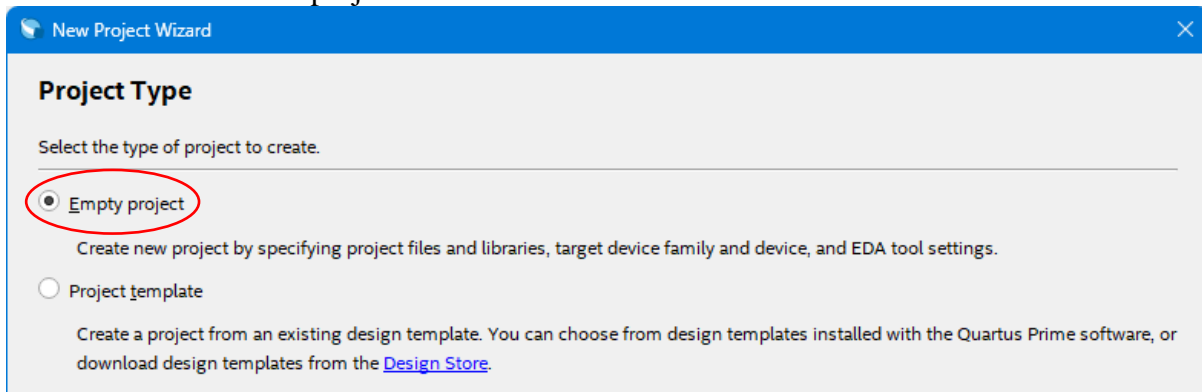
What is the name of this project?

lab1

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

sw2display

Choose to create a new project



**New Project Wizard**

**Project Type**

Select the type of project to create.

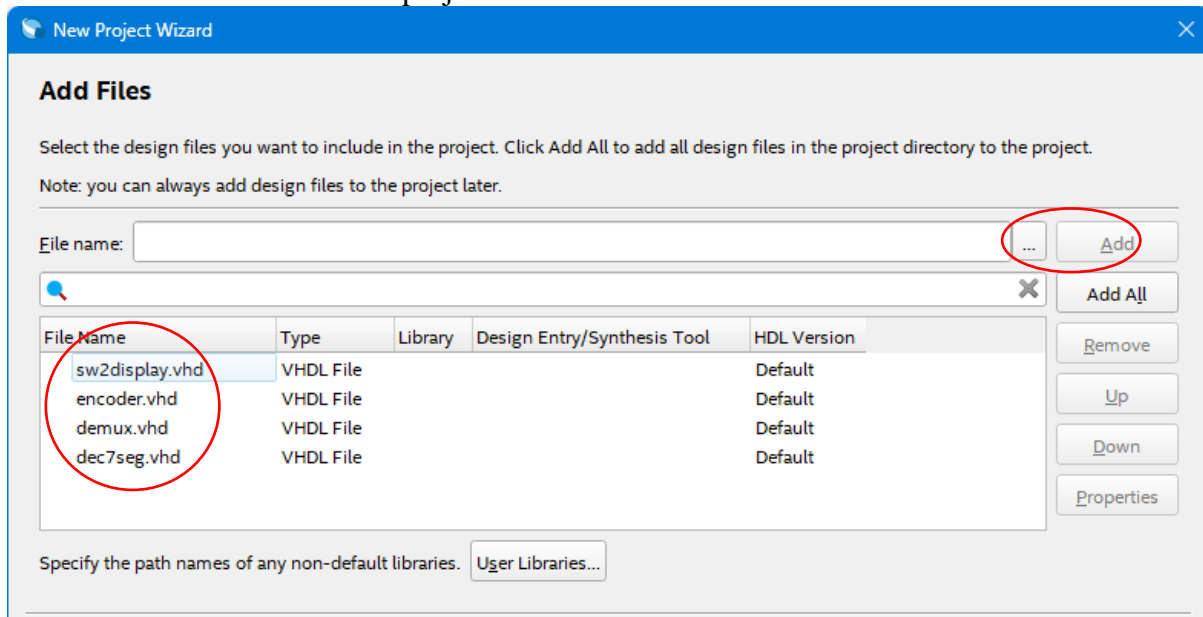
Empty project

Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.

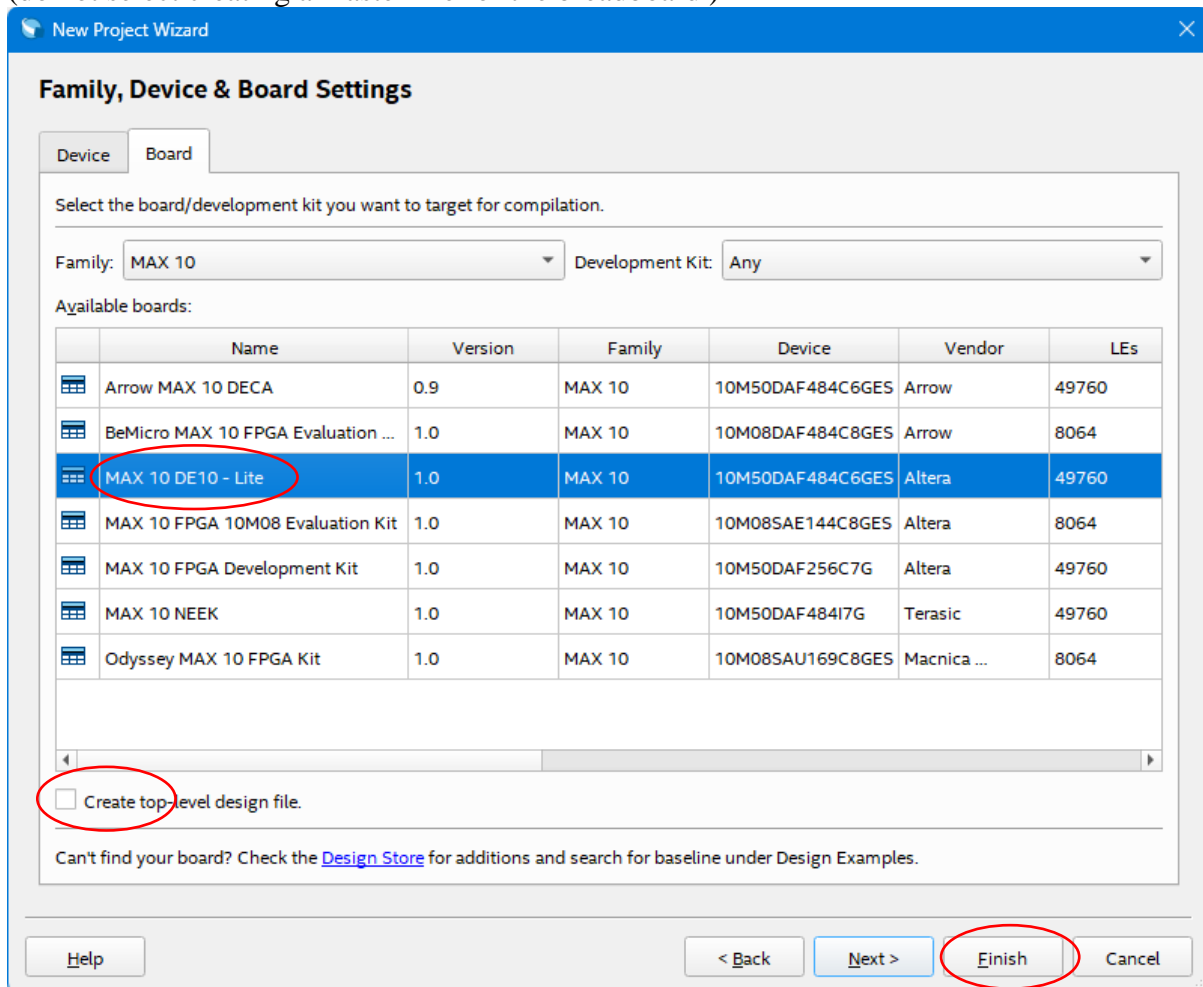
Project template

Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the [Design Store](#).

## Add VHDL source files to the project

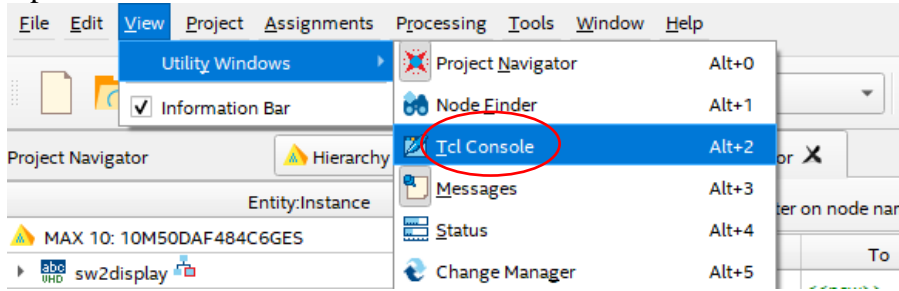


## Select the type of breadboard from the **Board** tab (do not select creating a master file for the breadboard)

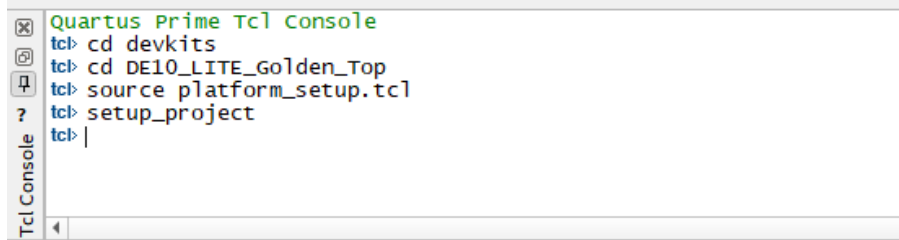


## 2. Pin configuration

Open the Tcl console



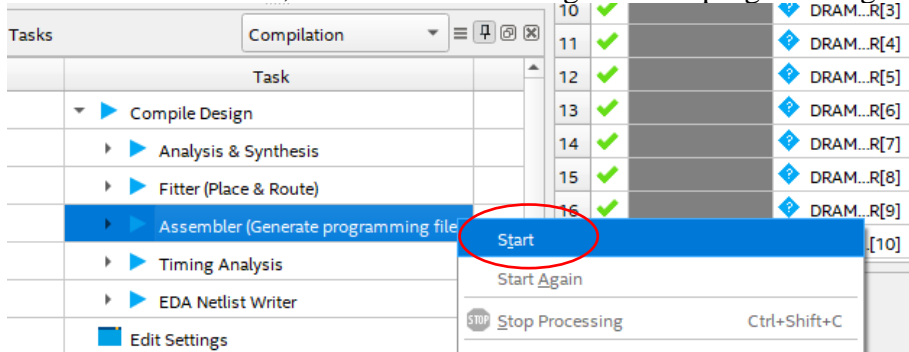
Go to the `./devkits/DE10_LITE_Golden_Top` directory and run the configuration script



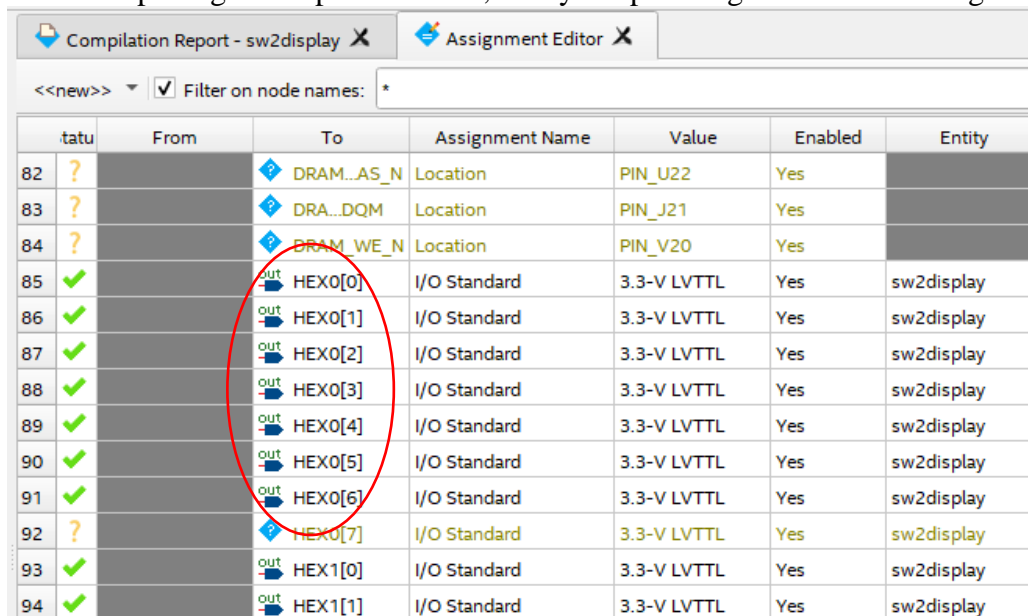
If the ports in the main unit match the names on the prototype board, the assignment of the IC pin numbers has been done automatically.

## 3. Project build

In the Tasks window, run the command to generate a programming file



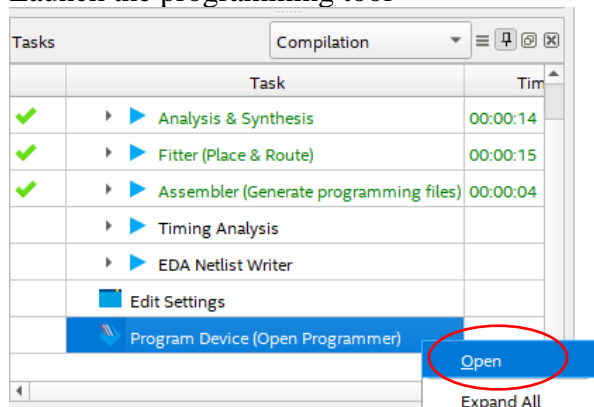
After completing the implementation, verify the pin assignment in the Assignment Editor window



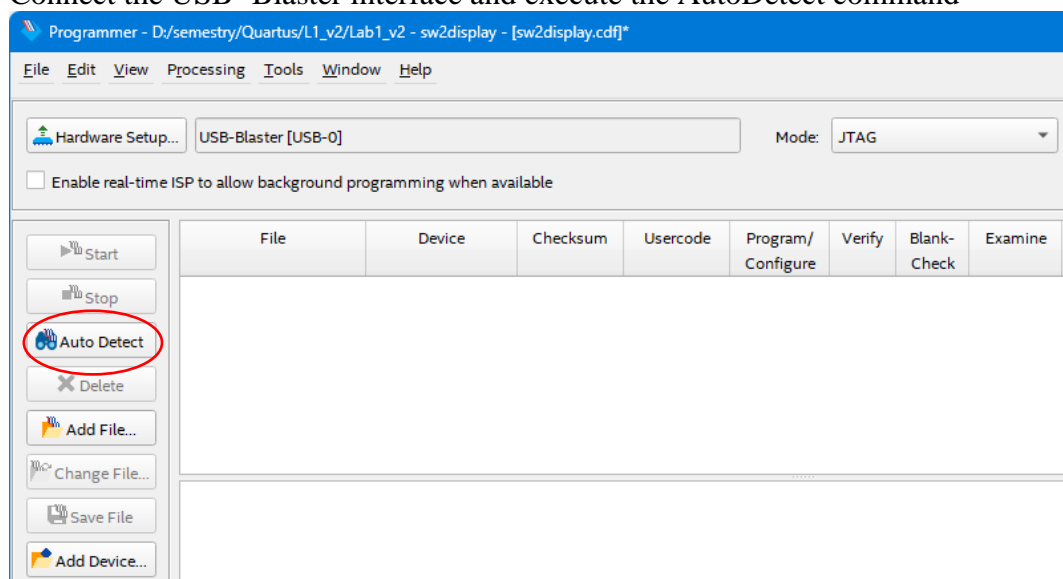
tatu	From	To	Assignment Name	Value	Enabled	Entity
82	?	DRAM..AS_N	Location	PIN_U22	Yes	
83	?	DRA...DQM	Location	PIN_J21	Yes	
84	?	DRAM_WE_N	Location	PIN_V20	Yes	
85	✓	HEX0[0]	I/O Standard	3.3-V LVTTTL	Yes	sw2display
86	✓	HEX0[1]	I/O Standard	3.3-V LVTTTL	Yes	sw2display
87	✓	HEX0[2]	I/O Standard	3.3-V LVTTTL	Yes	sw2display
88	✓	HEX0[3]	I/O Standard	3.3-V LVTTTL	Yes	sw2display
89	✓	HEX0[4]	I/O Standard	3.3-V LVTTTL	Yes	sw2display
90	✓	HEX0[5]	I/O Standard	3.3-V LVTTTL	Yes	sw2display
91	✓	HEX0[6]	I/O Standard	3.3-V LVTTTL	Yes	sw2display
92	?	HEX0[7]	I/O Standard	3.3-V LVTTTL	Yes	sw2display
93	✓	HEX1[0]	I/O Standard	3.3-V LVTTTL	Yes	sw2display
94	✓	HEX1[1]	I/O Standard	3.3-V LVTTTL	Yes	sw2display

## 4. Disc programming

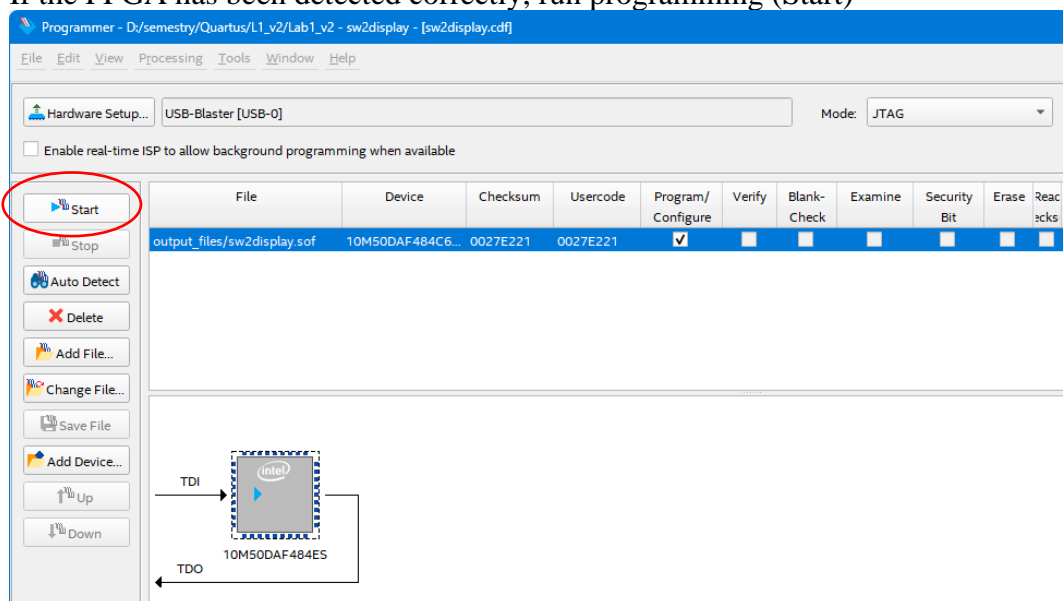
Launch the programming tool



Connect the USB- Blaster interface and execute the AutoDetect command



If the FPGA has been detected correctly, run programming (Start)



Test the operation of the system using the SW switches