

Quartus Prime – quick start

1. Preparing the project

Launch Quartus Prime In the start window, select New Project Wizard



Select a working directory, enter the project name and the name of the main project unit

S New Project Wizard	\times
Directory, Name, Top-Level Entity	
What is the <u>w</u> orking directory for this project?	
D:/semestry/Quartus/lab1 .	
What is the name of this project?	
lab1	
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.	e
sw2display .	

Choose to create a new project

🕞 New Project Wizard	×
Project Type	
Select the type of project to create.	
Empty project	
Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.	
O Project <u>t</u> emplate	
Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, download design templates from the <u>Design Store</u> .	or

Add VHDL source files to the project

aa riies					
elect the design files yo	u want to includ	e in the pro	ject. Click Add All to add all desi	gn files in the project director	y to the project.
ote: you can always add	l design files to t	he project	later.		
I					
le name:					
\					X Add A
ile Mame	Туре	Library	Design Entry/Synthesis Tool	HDL Version	Remov
sw2display.vhd	VHDL File			Default	
encoder.vhd	VHDL File			Default	Up
demux.vhd	VHDL File			Default	Down
dec7seg.vhd	VHDL File			Default	Down
					Propert

Select the type of breadboard from the **Board** tab (do not select creating a master file for the breadboard)

Select	t the board/development kit you want	to target for compil	ation.			
Famil	y: MAX 10	•	Development Kit:	Any		•
A <u>v</u> aila	able boards:					
	Name	Version	Family	Device	Vendor	LEs
==	Arrow MAX 10 DECA	0.9	MAX 10	10M50DAF484C6GES	Arrow	49760
■	BeMicro MAX 10 FPGA Evaluation	1.0	MAX 10	10M08DAF484C8GES	Arrow	8064
• (MAX 10 DE10 - Lite	1.0	MAX 10	10M50DAF484C6GES	Altera	49760
	MAX 10 FPGA 10M08 Evaluation Kit	1.0	MAX 10	10M08SAE144C8GES	Altera	8064
==	MAX 10 FPGA Development Kit	1.0	MAX 10	10M50DAF256C7G	Altera	49760
==	MAX 10 NEEK	1.0	MAX 10	10M50DAF484I7G	Terasic	49760
	Odyssey MAX 10 FPGA Kit	1.0	MAX 10	10M08SAU169C8GES	Macnica	8064
Cr Can't	reate top level design file. find your board? Check the <u>Design Sto</u>	ere for additions and	d search for baselin	e under Design Exampl	es.	Þ

2. Pin configuration

Open inc	- 10	conso	le le					
<u>F</u> ile <u>E</u> dit	<u>V</u> iew	<u>P</u> roject	<u>A</u> ssignments	P <u>r</u> ocessing	<u>T</u> ools	<u>W</u> indow	<u>H</u> elp	
Utility Windows >			💢 Project	<u>N</u> avigat	or	Alt+0		
	nformatior	n Bar	Node E	inder		Alt+1	· ·	
Project Navigator		A Hierarchy	📕 <u>I</u> cl Cor	nsole		Alt+2	or 🗙	
Entity:Instance				Messag	ges		Alt+3	ter on node nan
A MAX 10: 10M50DAF484C6GES			E Status			Alt+4		
▶ Bbg sw2display 👛			🌏 Change	e Manage	er	Alt+5	10	

Go to the ./devkits/DE10_LITE_Golden_Top directory and run the configuration script



If the ports in the main unit match the names on the prototype board, the assignment of the IC pin numbers has been done automatically.

3. Project build

In the Tasks window, run the command to generate a programming file

		(10			V DRAMR[3]
Tasks		Compilation = 🖛 🗇 🖗				11	~		ORAMR[4]
		Task			*	12	-		ORAMR[5]
	🝷 🕨 Compile Desig	gn .				13	~		ORAMR[6]
	Analysis &	Synthesis				14	~		DRAMR[7]
	Fitter (Place)	e & Route)				15	~		DRAMR[8]
	🕨 🕨 Assemble	r (Generate progran	nming file	Sta		16	\leq		ORAMR[9]
	🕨 🕨 Timing An	^	Sta	rt A	gain			.[10]	
	🕨 🕨 EDA Netlis	t Writer				Sam			
	Edit Settings		Sto Sto	Ctrl+Shift+C					

After completing the implementation, verify the pin assignment in the Assignment Editor window

Ç	Compilation Report - sw2display 🗙 🎸 Assignment Editor 🗙										
<<	< <new>> 🔻 🔽 Filter on node names: *</new>										
	tatu	From	То	Assignment Name	Value	Enabled	Entity				
82	?		DRAMAS_N	Location	PIN_U22	Yes					
83	?		🔷 DRADQM	Location	PIN_J21	Yes					
84	?		STAM WE_N	Location	PIN_V20	Yes					
85	~		HEXO[0]	I/O Standard	3.3-V LVTTL	Yes	sw2display				
86	~	/	HEXO[1]	I/O Standard	3.3-V LVTTL	Yes	sw2display				
87	~		HEXO[2]	I/O Standard	3.3-V LVTTL	Yes	sw2display				
88	~		HEXO[3]	I/O Standard	3.3-V LVTTL	Yes	sw2display				
89	~		HEXO[4]	I/O Standard	3.3-V LVTTL	Yes	sw2display				
90	~		HEXO[5]	I/O Standard	3.3-V LVTTL	Yes	sw2display				
91	~	1	HEXO[6]	I/O Standard	3.3-V LVTTL	Yes	sw2display				
92	?			I/O Standard	3.3-V LVTTL	Yes	sw2display				
93	~		HEX1[0]	I/O Standard	3.3-V LVTTL	Yes	sw2display				
94	~		HEX1[1]	I/O Standard	3.3-V LVTTL	Yes	sw2display				

4. Disc programming

Launch the programming tool

Tasks	Compilation 👻	= ₽ Ø ×
	Task	Tim
 Image: A second s	🕨 🕨 Analysis & Synthesis	00:00:14
 Image: A second s	Fitter (Place & Route)	00:00:15
 Image: A second s	Assembler (Generate programming files)	00:00:04
	🕨 🕨 Timing Analysis	
	EDA Netlist Writer	
	Edit Settings	
	Nogram Device (Open Programmer)	
		<u>O</u> pen
4		Expand All

Connect the USB- Blaster interface and execute the AutoDetect command

Programmer - D:/se	emestry/Quartus/L1_v2/Lat	o1_v2 - sw2display	- [sw2display.cdf]	*				
<u>File E</u> dit <u>V</u> iew P <u>r</u>	ocessing <u>T</u> ools <u>W</u> indo	w <u>H</u> elp						
Hardware Setup	USB-Blaster [USB-0]	Mode:	JTAG		¥			
► ^V Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine
Auto Detect								
X Delete								
Change File								
Save File								
Add Device								

If the FPGA has been detected correctly, run programming (Start)

👋 Programı	mer - D:/se	emestry/Quartus/L1_v2/Lab1_v2	- sw2display - [sw2di	splay.cdf]									
<u>File</u> <u>E</u> dit	View Pro	ocessing <u>T</u> ools <u>W</u> indow <u>F</u>	delp										
Hardwar	Hardware Setup USB-Blaster [USB-0] Enable real-time ISP to allow background programming when available									Mode: JTAG			
Star		File	Device	Checksum	Usercode	Program/	Verify	Blank-	Examine	Security	Erase	Reac	
		output files/sw2display.sof	10M50DAF484C6	0027E221	0027E221	Configure		Check		Bit		ecks	C
stop													
Auto De	etect												
X Delet	te												
Add Fi	le												
No. Change	File												
Save F	ile												
Add Dev The Up	n	TDI 10M50DAF484ES											

Test the operation of the system using the SW switches