Digital Logic
Design with FPGA

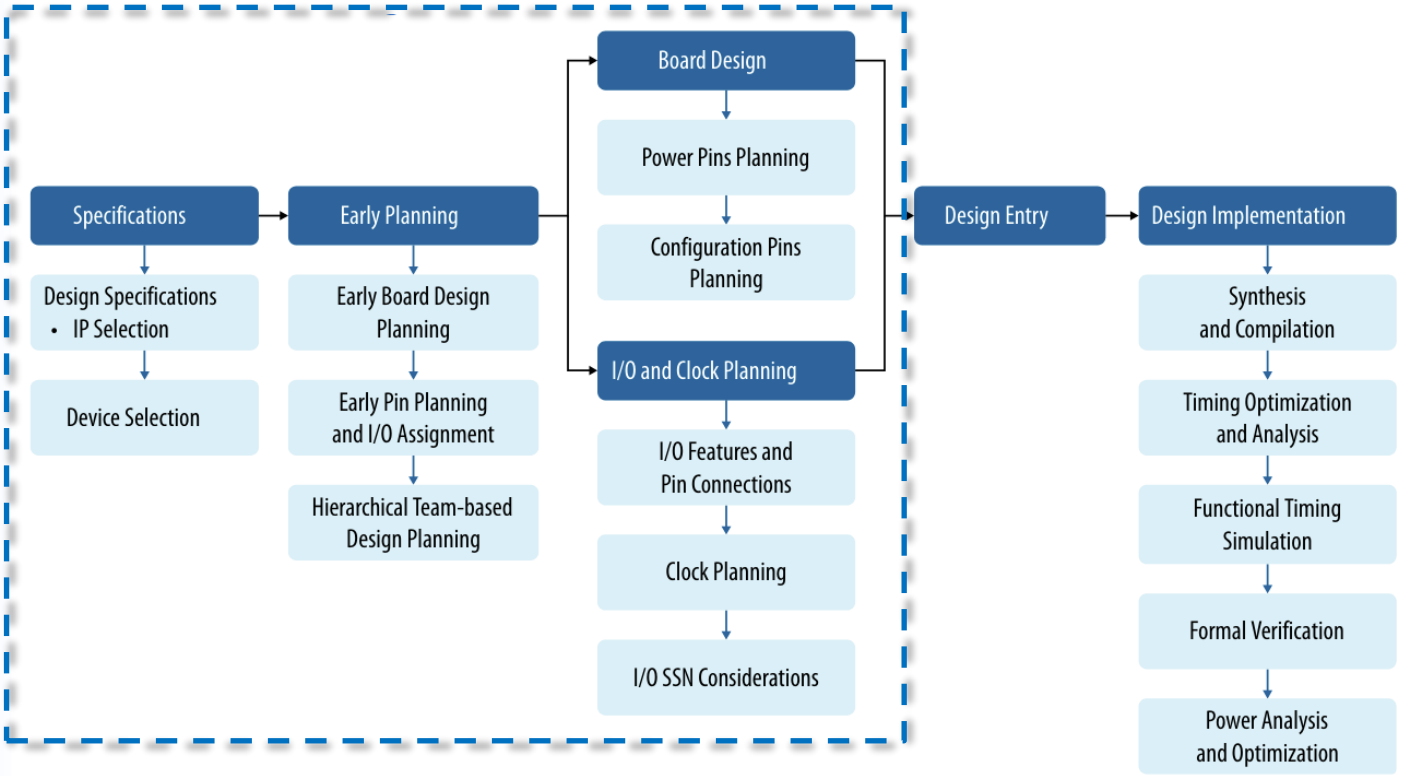
# Design Flow with Quartus

## Design Constraints, I/O Planning

# Outline

- Synthesis & Fitting Control
- Design constraints
- Assignment editor
- I/O assignments
- Pin planner
- I/O assignment validation

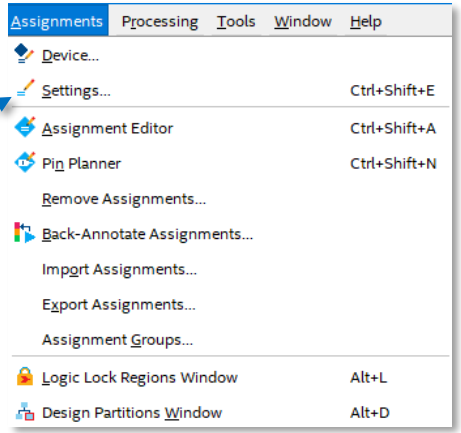
# Intel MAX10 Design Flow

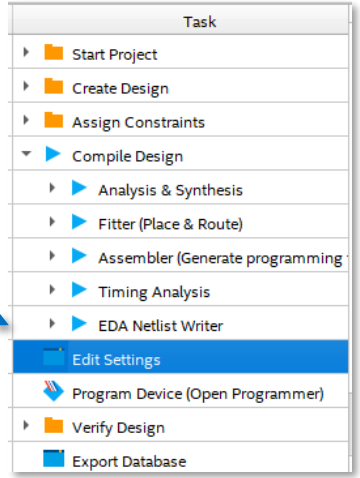



source: https://www.intel.com/content/www/us/en/docs/programmable/683196/current/fpga-design-guidelines-34288.html

# Synthesis & Fitting Control

- Controlled using two methods
  - Settings: project-wide switches
  - Assignments: individual entity/node controls
- Both accessed in Assignments menu or Tasks window




- Stored in **.qsf** file for project/revision
- Timing constraints stored in separate **.sdc** file

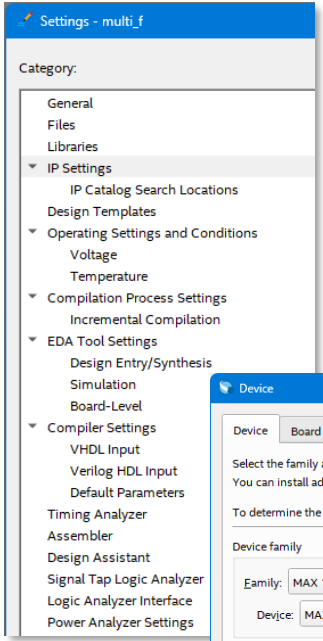


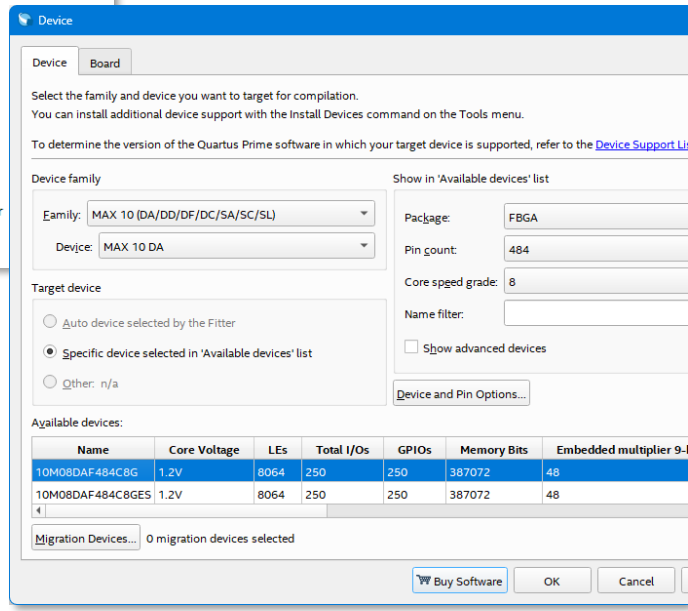
source: https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-software/fpga-development-tools-support.html

# Settings & Assignments

- Project-wide switches that affect entire design
- Settings Dialog Box:
  - Top-level entity
  - Add/remove files
  - Libraries
  - Compiler settings
  - EDA tool settings
  - Fitter settings
  - Timing Analyzer settings
  - Power analysis settings

***Tcl***: `set_global_assignment -name <assignment_name> <value>`




- Device Dialog Box
  - Choose device family & family category

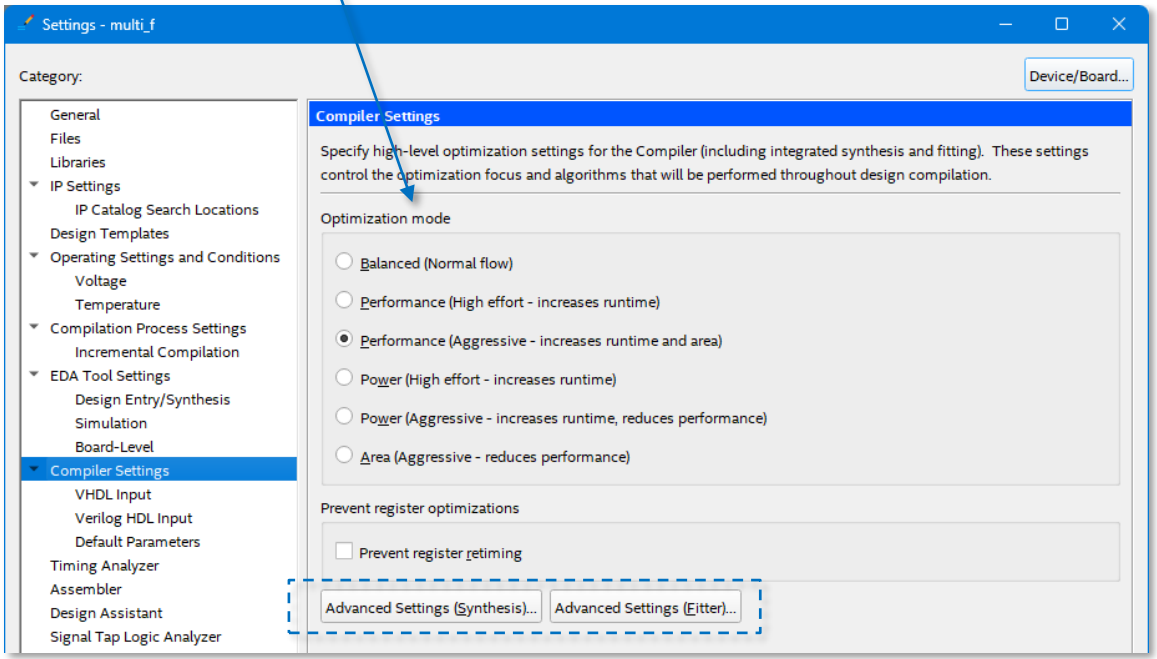
***Tcl***: `set_global_assignment -name FAMILY "device family name"`
***Tcl***: `set_global_assignment -name DEVICE <part_number>`

source: https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-software/fpga-development-tools-support.html

# Settings & Assignments

Example: Consolidated Compiler Optimization Settings

- Choose general options for how compiler should optimize design
- Set specific optimization features under **Advanced Settings** buttons



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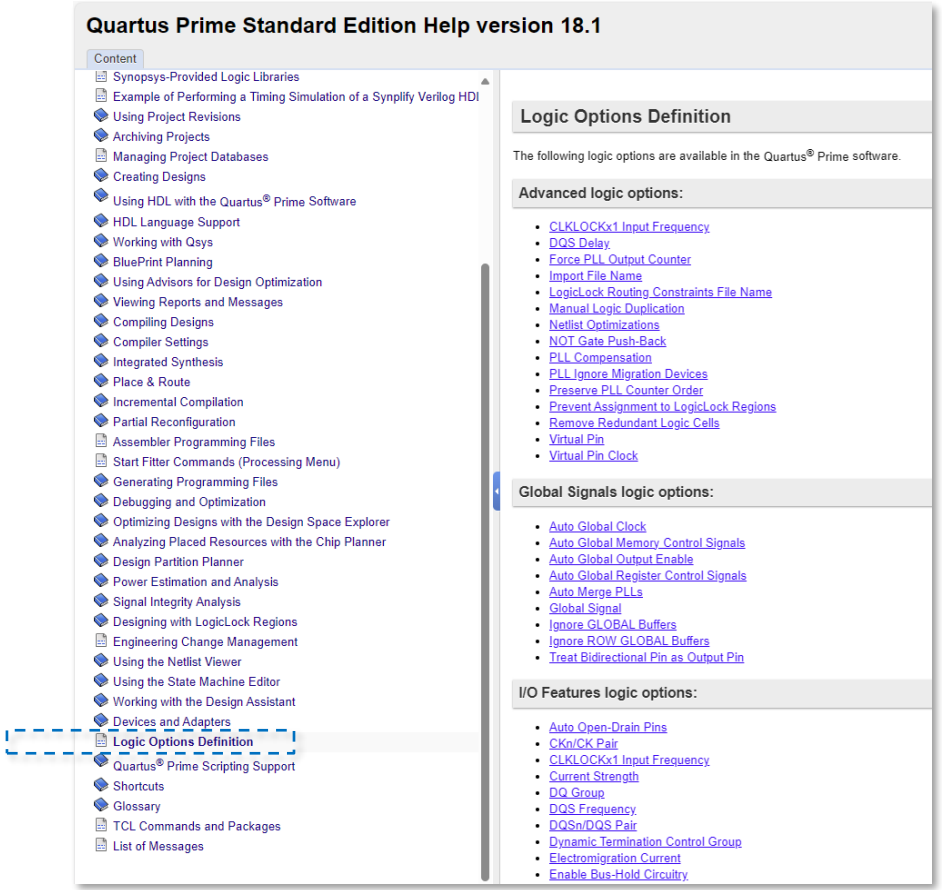
# Settings & Assignments

(aka Logic Options, Constraints)

- Individual switches applied
  - I/O
  - Internal nodes
  - Hierarchical blocks (design entities)
- Assignment Editor manages assignments
- Stored in .**qsf** file
- Must perform analysis & elaboration

- Available Logic Options (Assignments)
  - Links to all available assignments organized by category



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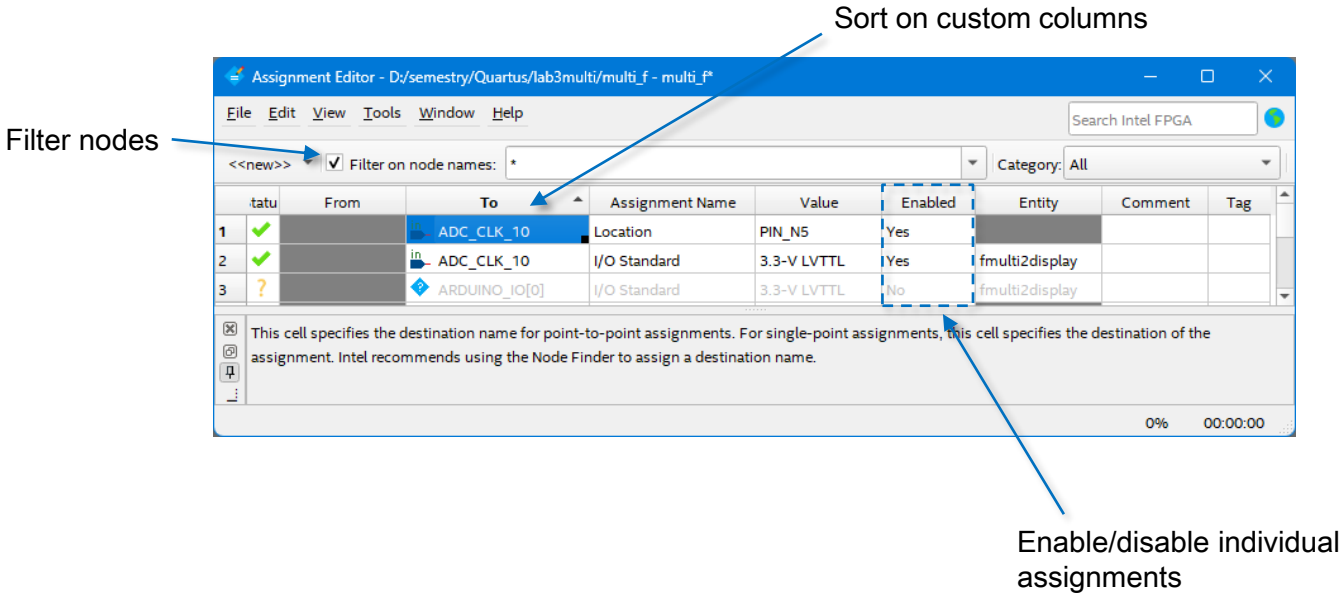
# Assignment Editor

Provides spreadsheet assignment entry & display

- Copy & paste support
- Multi-cell editing
- Assignments menu, toolbar, or Tasks window



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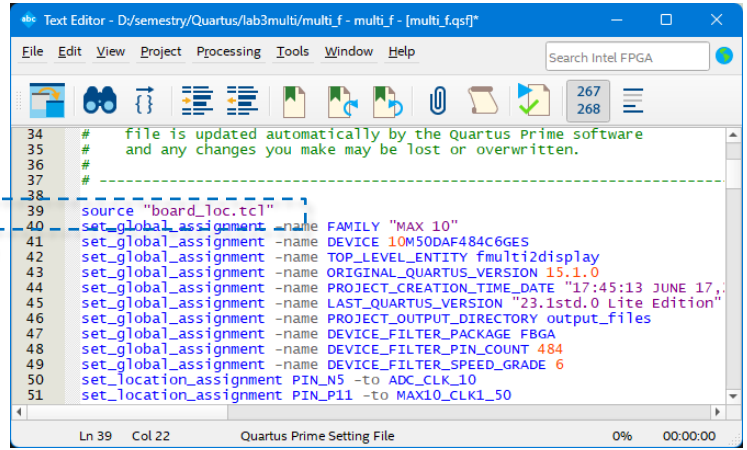
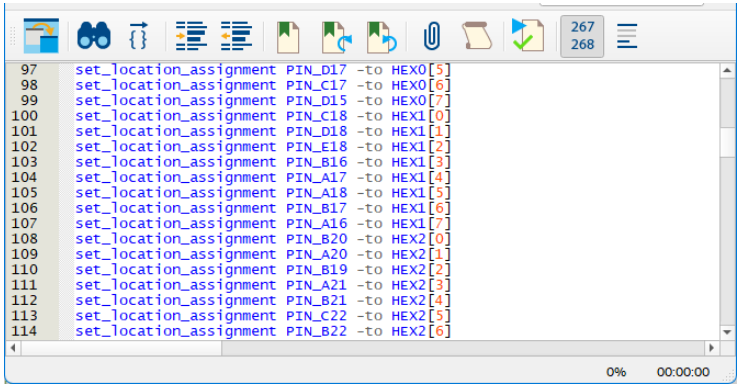
# Design constraints - scripting

.**qsf** editing and scripting

- Type pin-related assignment directly into .**qsf**
- Type pin-related assignment into separate Tcl file
  - Source Tcl into project .**qsf**
  - Execute Tcl to write assignments into .**qsf**



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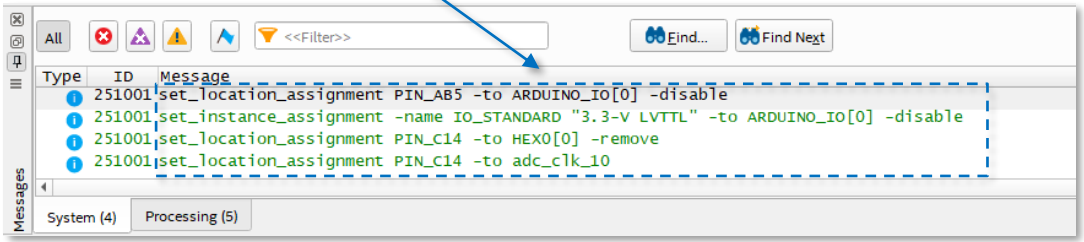
# Design constraints – Tcl commands

Equivalent Tcl commands displayed as assignments are entered

- Manually copy to create Tcl scripts
- Export command (**File** menu) writes all assignments to a Tcl file

**Messages** window



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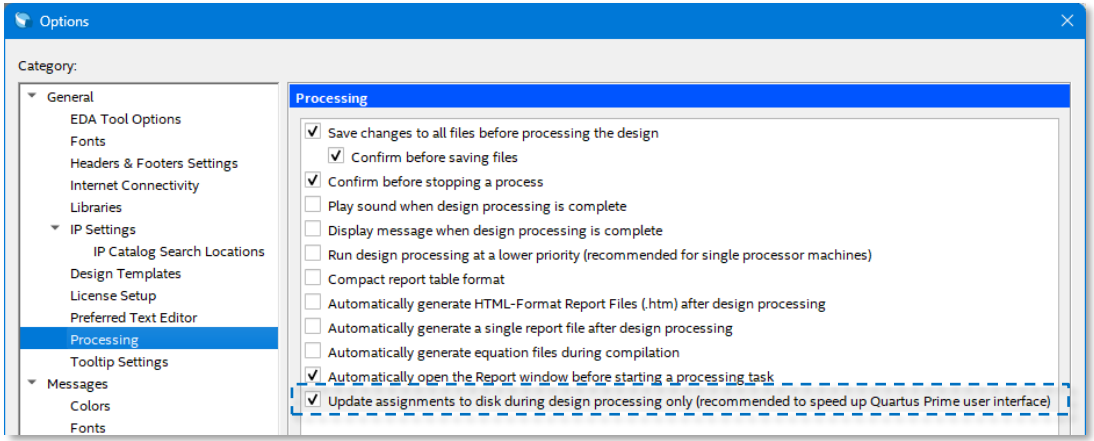
# Updating .qsf File

- By default, .**qsf** not updated automatically when constraint entered
- .**qsf** updated only when
  - Project is saved or closed (File menu)
  - Assignment Editor is saved or closed
  - Beginning of any processing task (e.g. compilation)
  - Any IP parameter editing tool is launched
  - Changing revisions




- Change behavior to update assignments immediately (Tools menu → Options → General → Processing)
  - May impact software performance slightly due to file accesses



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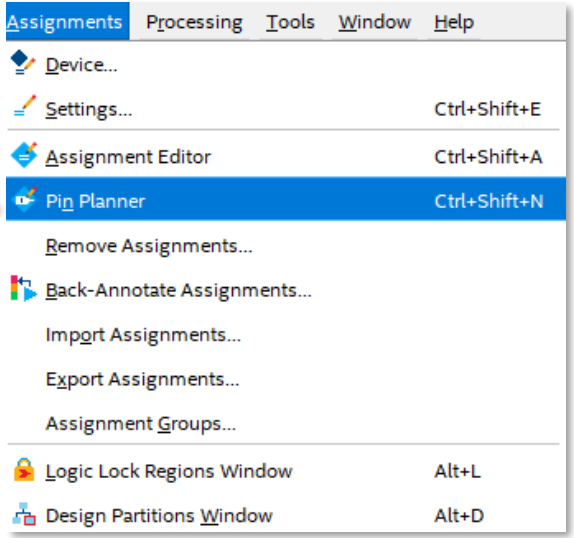
# I/O assignments

- I/O Planning need
  - I/O standards increasing in complexity
  - FPGA/CPLD I/O structure increasing in complexity
  - PCB development performed simultaneously with FPGA design
  - Pin assignments need to be verified earlier in design cycle

- Creating I/O-Related Assignments
  - Pin Planner
  - Import from spreadsheet in .**csv** format
  - Type directly into .**qsf** file
  - Directly in HDL code
  - Scripting



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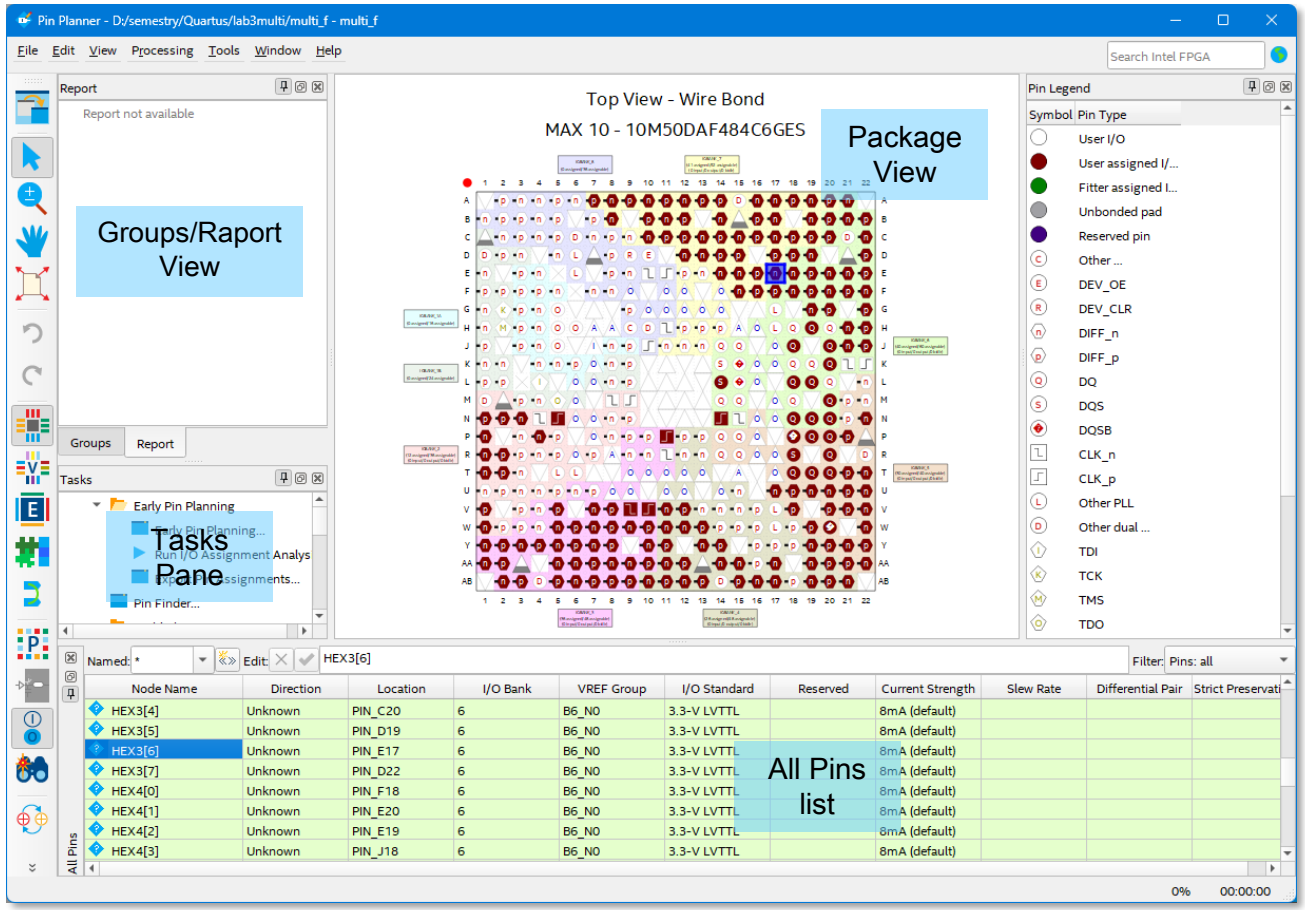
# Pin Planner

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# Pin Planner

- Package View
  - Displays graphical representation of chip package
  - Locate, make, or edit I/O assignments
- All Pins list
  - Displays I/O pins (signals) in design
  - Edit pin assignments
- Groups list
  - Similar to All Pins list displaying only groups & buses
  - Make bus and group assignments
  - Create new user-defined groups
- Tasks pane
  - Perform tasks such as Early Pin Planning and pin highlight reports
- Report Pane
  - Quickly enable/disable reports generated in the Tasks pane



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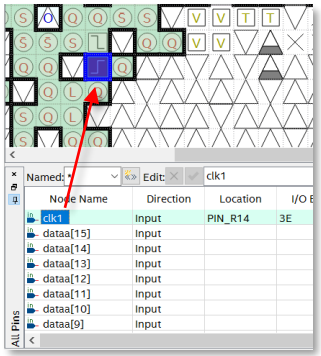
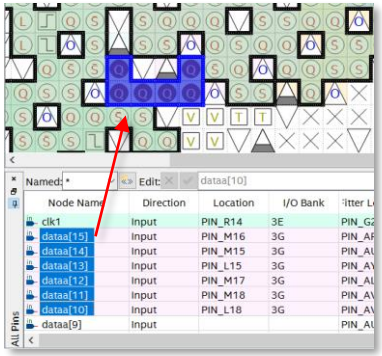
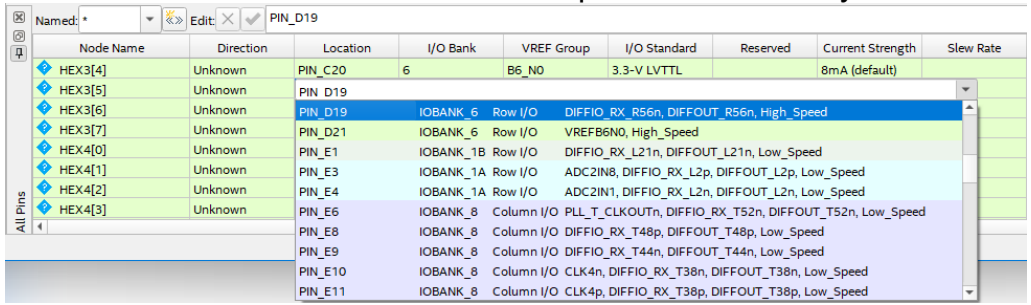
# Pin Planner

- Assigning Pin Locations
  - Drag & drop single top-level I/O signal/pin
  - Drag & drop multiple highlighted pins or buses




  - Select available locations from list of pins color-coded by I/O bank



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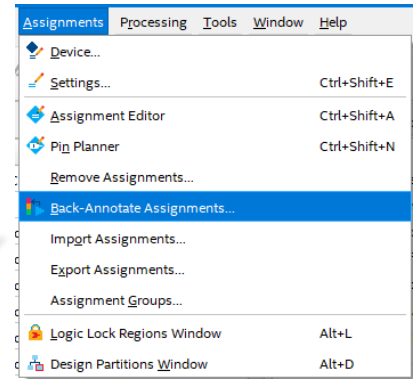
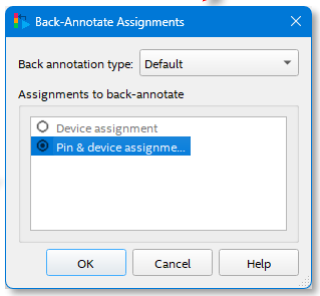
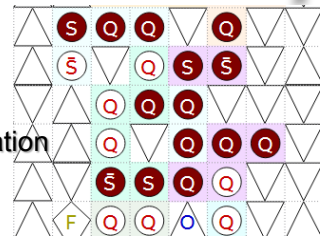
# Pin Planner

- Back-Annotation
  - Use to lock Fitter-chosen pin assignments for future compilations
    - Copies device & resource locations chosen by fitter into .**qsf** file
      - Pins
      - Logic
    - Routing
  - “Locks down” locations in Pin Planner




Green/brown pattern indicates back-annotation





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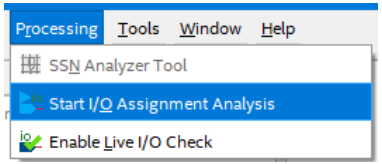
# Pin Planner

Verifying I/O Assignments

- I/O Assignment Analysis
  - Checks legality of all I/O assignments without full compilation
- Minimal requirements for running
  - I/O declaration
    - HDL port declaration
    - Reserved pin
  - Pin-related assignments
    - I/O standard
    - Current strength
    - Pin location (pin, bank, edge)
    - Toggle rate
- Pin Planner Processing menu → Start I/O Assignment Analysis

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# Pin Planner

I/O Rules Checked

- No internal logic
  - Checks I/O locations & constraints with respect to other I/O & I/O banks
  - e.g. Each I/O bank supports a single VCCIO
- I/O connected to logic
  - Checks I/O locations & constraints with respect to other I/O, I/O banks, & internal resources
  - e.g. PLL must be driven by a dedicated clock input pin
- Note: When working with design files, synthesize design before running I/O Assignment Analysis



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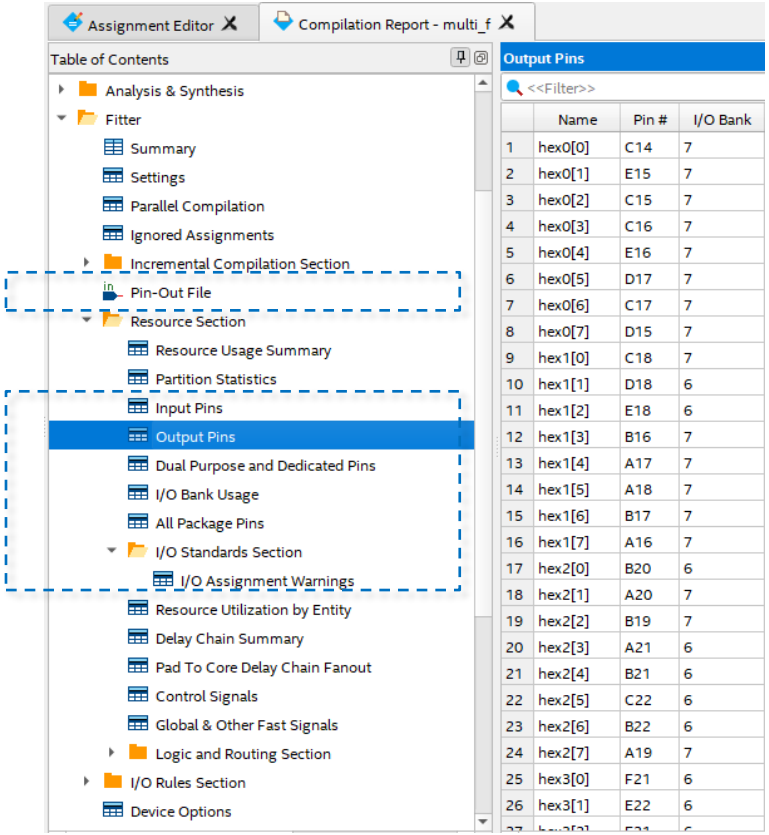
# I/O Assignment Analysis Output

Messages on I/O assignment issues

- Compiler assumptions
- Device & pin migration issues
- I/O bank voltages & standards

Validating I/O Pin-out

- **Completed design**
  - Run full compilation
  - Enable option to Run I/O Assignment Analysis before compilation
    (Settings dialog box → Compilation Process Settings)
- **Incomplete design** with completed top-level design file
  - Add I/O-related IP cores and instantiate, even if final connections are not complete
  - Run I/O Assignment Analysis on design

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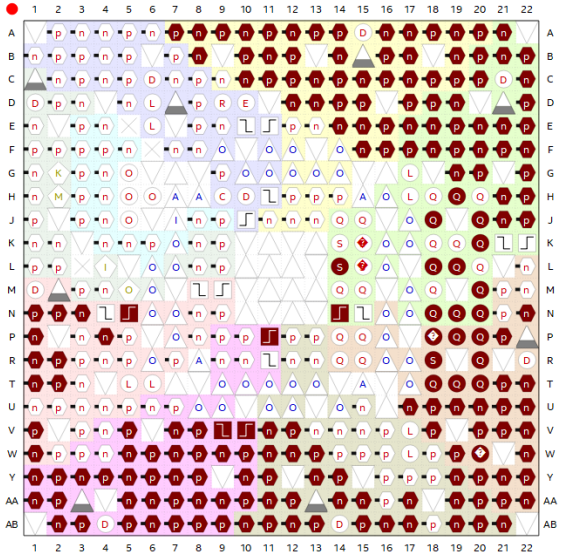
# I/O Planning Summary

- Pin assignments can be performed in many ways, graphically & by means of text files
- The Pin Planner provides an easy-to-use graphical method for creating and managing pin assignments
- The Interface Planner combines I/O interface resource assignment with on-the-fly legality checking
- I/O Assignment Analysis helps validate a device pin-out without performing a full compilation
- Pin validation can be completed during any point in design development



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