



Digital Logic  
Design with FPGA

# Design Flow with Quartus

Design Constraints, I/O Planning

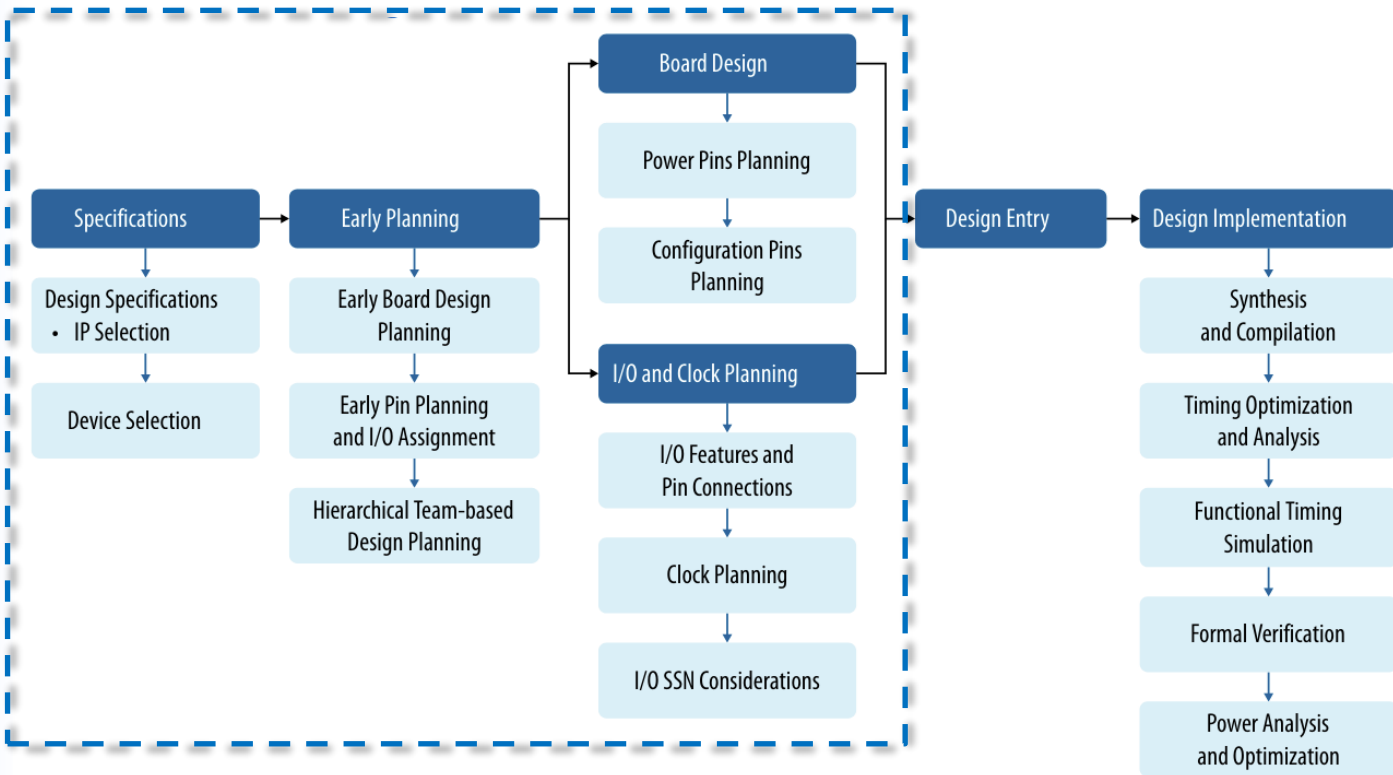


# Outline

- Synthesis & Fitting Control
- Design constraints
- Assignment editor
- I/O assignments
- Pin planner
- I/O assignment validation



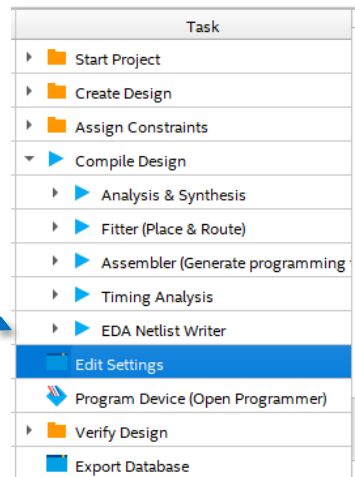
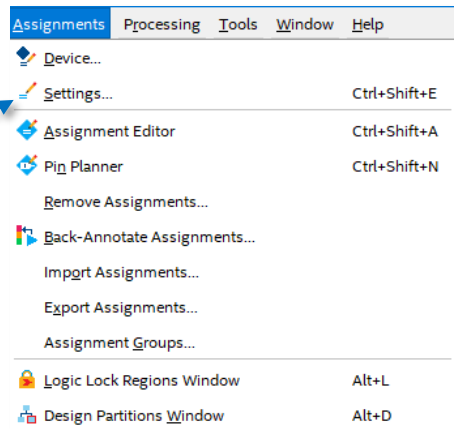
# Intel MAX10 Design Flow





# Synthesis & Fitting Control

- Controlled using two methods
  - **Settings**: project-wide switches
  - **Assignments**: individual entity/node controls
- Both accessed in Assignments menu or Tasks window



- Stored in **.qsf** file for project/revision
- **Timing constraints** stored in separate **.sdc** file



# Settings & Assignments

- Project-wide switches that affect entire design
- Settings Dialog Box:
  - Top-level entity
  - Add/remove files
  - Libraries
  - Compiler settings
  - EDA tool settings
  - Fitter settings
  - Timing Analyzer settings
  - Power analysis settings

```
Tcl: set_global_assignment -name <assignment_name> <value>
```

- Device Dialog Box
  - Choose device family & family category

```
Tcl: set_global_assignment -name FAMILY "device family name"
```

```
Tcl: set_global_assignment -name DEVICE <part_number>
```

Settings - multi\_f

Category:

- General
- Files
- Libraries
- IP Settings
  - IP Catalog Search Locations
- Design Templates
- Operating Settings and Conditions
  - Voltage
  - Temperature
- Compilation Process Settings
  - Incremental Compilation
- EDA Tool Settings
  - Design Entry/Synthesis
  - Simulation
  - Board-Level
- Compiler Settings
  - VHDL Input
  - Verilog HDL Input
  - Default Parameters
- Timing Analyzer
- Assembler
- Design Assistant
- Signal Tap Logic Analyzer
- Logic Analyzer Interface
- Power Analyzer Settings

Device

Device Board

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#).

Device family: MAX 10 (DA/DD/DF/DC/SA/SC/SL) Show in 'Available devices' list

Family: MAX 10 (DA/DD/DF/DC/SA/SC/SL) Package: FBGA

Device: MAX 10 DA Pin count: 484

Target device: Core speed grade: 8

Auto device selected by the Fitter  
 Specific device selected in 'Available devices' list  
 Other: n/a

Name filter:

Show advanced devices

Device and Pin Options...

Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier 9-
10M08DAF484C8G	1.2V	8064	250	250	387072	48
10M08DAF484C8GES	1.2V	8064	250	250	387072	48

Migration Devices... 0 migration devices selected

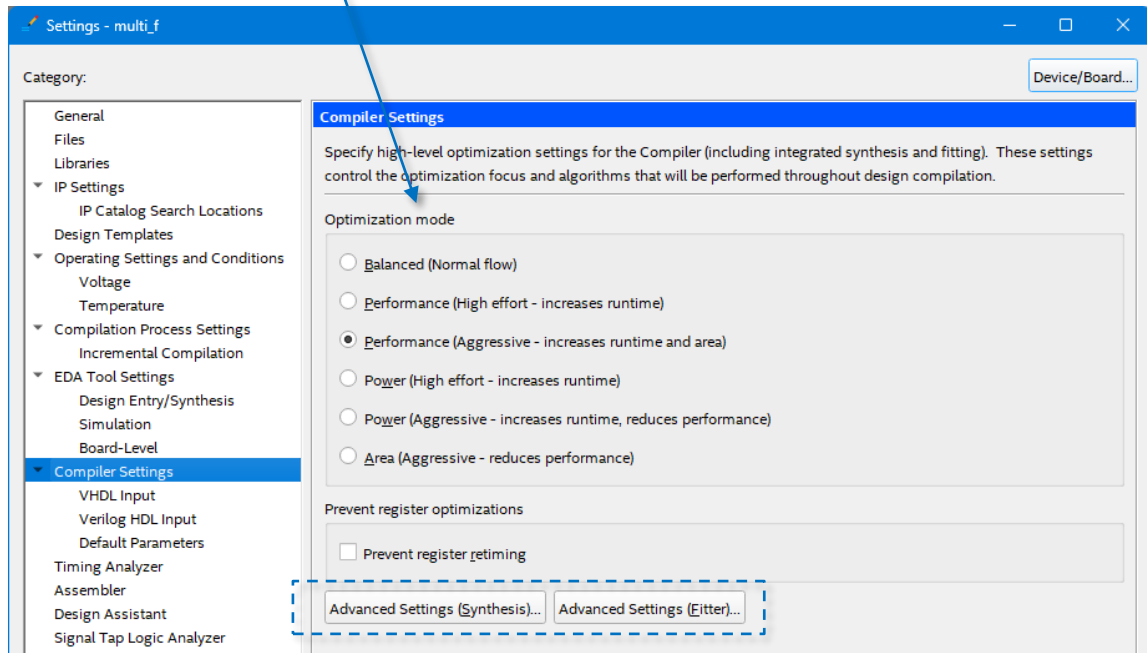
Buy Software OK Cancel



# Settings & Assignments

Example: Consolidated Compiler Optimization Settings

- Choose general options for how compiler should optimize design
- Set specific optimization features under **Advanced Settings** buttons





# Settings & Assignments

(aka Logic Options, [Constraints](#))

- Individual switches applied
  - I/O
  - Internal nodes
  - Hierarchical blocks (design entities)
- Assignment Editor manages assignments
- Stored in **.qsf** file
- Must perform analysis & elaboration
  
- Available Logic Options (Assignments)
  - Links to all available assignments organized by category

**Quartus Prime Standard Edition Help version 18.1**

Content

- Synopsys-Provided Logic Libraries
- Example of Performing a Timing Simulation of a Synplify Verilog HDI
- Using Project Revisions
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- HDL Language Support
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- Devices and Adapters
- Logic Options Definition**
- Quartus® Prime Scripting Support
- Shortcuts
- Glossary
- TCL Commands and Packages
- List of Messages

### Logic Options Definition

The following logic options are available in the Quartus® Prime software.

#### Advanced logic options:

- [CLKLOCKx1 Input Frequency](#)
- [DQS Delay](#)
- [Force PLL Output Counter](#)
- [Import File Name](#)
- [LogicLock Routing Constraints File Name](#)
- [Manual Logic Duplication](#)
- [Netlist Optimizations](#)
- [NOT Gate Push-Back](#)
- [PLL Compensation](#)
- [PLL Ignore Migration Devices](#)
- [Preserve PLL Counter Order](#)
- [Prevent Assignment to LogicLock Regions](#)
- [Remove Redundant Logic Cells](#)
- [Virtual Pin](#)
- [Virtual Pin Clock](#)

#### Global Signals logic options:

- [Auto Global Clock](#)
- [Auto Global Memory Control Signals](#)
- [Auto Global Output Enable](#)
- [Auto Global Register Control Signals](#)
- [Auto Merge PLLs](#)
- [Global Signal](#)
- [Ignore GLOBAL Buffers](#)
- [Ignore ROW GLOBAL Buffers](#)
- [Treat Bidirectional Pin as Output Pin](#)

#### I/O Features logic options:

- [Auto Open-Drain Pins](#)
- [CKn/CK Pair](#)
- [CLKLOCKx1 Input Frequency](#)
- [Current Strength](#)
- [DQ Group](#)
- [DQS Frequency](#)
- [DQSn/DQS Pair](#)
- [Dynamic Termination Control Group](#)
- [Electromigration Current](#)
- [Enable Bus-Hold Circuitry](#)



# Assignment Editor

Provides spreadsheet assignment entry & display

- Copy & paste support
- Multi-cell editing
- Assignments menu, toolbar, or Tasks window

Sort on custom columns

Filter nodes

The screenshot shows the Assignment Editor window with a table of assignments. The table has columns: 'tatu', 'From', 'To', 'Assignment Name', 'Value', 'Enabled', 'Entity', 'Comment', and 'Tag'. Row 1 is selected. A dashed blue box highlights the 'Enabled' column for rows 2 and 3. A blue arrow points to the 'Filter on node names' checkbox, and another points to the 'Enabled' column header. A third arrow points to the 'Enabled' cell for row 3.

tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✓	ADC_CLK_10	Location	PIN_N5	Yes			
2	✓	ADC_CLK_10	I/O Standard	3.3-V LVTTTL	Yes	fmulti2display		
3	?	ARDUINO_IO[0]	I/O Standard	3.3-V LVTTTL	No	fmulti2display		

Enable/disable individual assignments





# Design constraints - scripting

.qsf editing and scripting

- Type pin-related assignment directly into .qsf
- Type pin-related assignment into separate Tcl file
  - Source Tcl into project .qsf
  - Execute Tcl to write assignments into .qsf

```
34 # file is updated automatically by the Quartus Prime software
35 # and any changes you make may be lost or overwritten.
36 #
37 # -----
38
39 source "board_loc.tcl"
40 set_global_assignment -name FAMILY "MAX 10"
41 set_global_assignment -name DEVICE 10M50DAF484C6GES
42 set_global_assignment -name TOP_LEVEL_ENTITY fmulti2display
43 set_global_assignment -name ORIGINAL_QUARTUS_VERSION 15.1.0
44 set_global_assignment -name PROJECT_CREATION_TIME_DATE "17:45:13 JUNE 17, 2015"
45 set_global_assignment -name LAST_QUARTUS_VERSION "23.1std.0 Lite Edition"
46 set_global_assignment -name PROJECT_OUTPUT_DIRECTORY output_files
47 set_global_assignment -name DEVICE_FILTER_PACKAGE FBGA
48 set_global_assignment -name DEVICE_FILTER_PIN_COUNT 484
49 set_global_assignment -name DEVICE_FILTER_SPEED_GRADE 6
50 set_location_assignment PIN_N5 -to ADC_CLK_I0
51 set_location_assignment PIN_P11 -to MAX10_CLK1_50
```

```
97 set_location_assignment PIN_D17 -to HEX0[5]
98 set_location_assignment PIN_C17 -to HEX0[6]
99 set_location_assignment PIN_D15 -to HEX0[7]
100 set_location_assignment PIN_C18 -to HEX1[0]
101 set_location_assignment PIN_D18 -to HEX1[1]
102 set_location_assignment PIN_E18 -to HEX1[2]
103 set_location_assignment PIN_B16 -to HEX1[3]
104 set_location_assignment PIN_A17 -to HEX1[4]
105 set_location_assignment PIN_A18 -to HEX1[5]
106 set_location_assignment PIN_B17 -to HEX1[6]
107 set_location_assignment PIN_A16 -to HEX1[7]
108 set_location_assignment PIN_B20 -to HEX2[0]
109 set_location_assignment PIN_A20 -to HEX2[1]
110 set_location_assignment PIN_B19 -to HEX2[2]
111 set_location_assignment PIN_A21 -to HEX2[3]
112 set_location_assignment PIN_B21 -to HEX2[4]
113 set_location_assignment PIN_C22 -to HEX2[5]
114 set_location_assignment PIN_B22 -to HEX2[6]
```

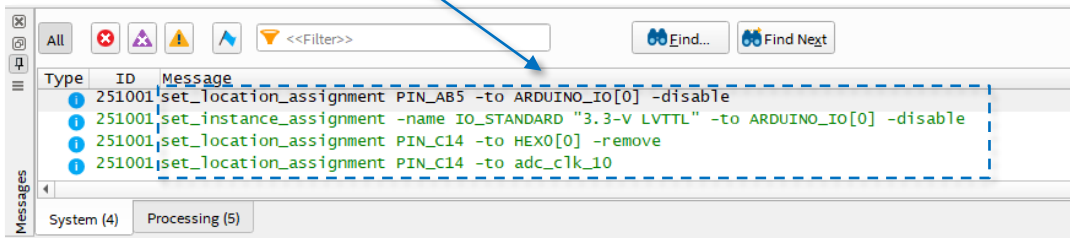


# Design constraints – Tcl commands

Equivalent Tcl commands displayed as assignments are entered

- ❑ Manually copy to create Tcl scripts
- ❑ Export command (**File** menu) writes all assignments to a Tcl file

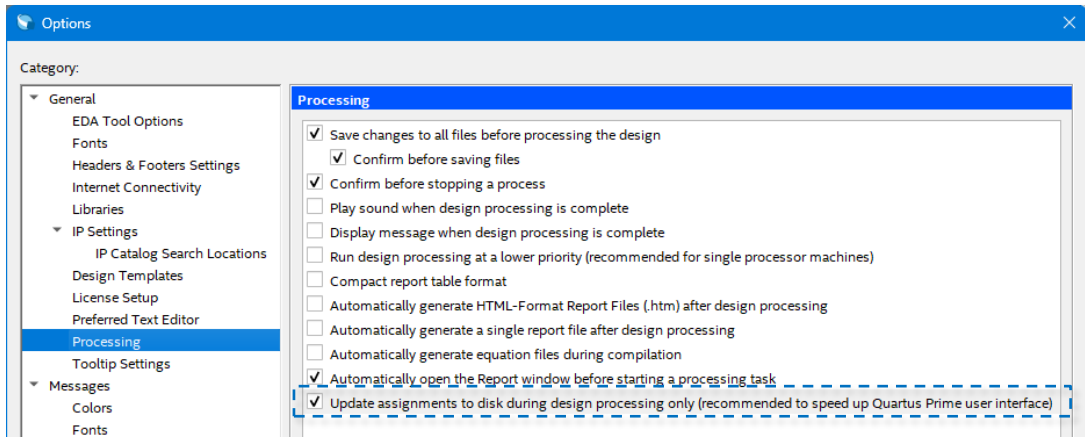
Messages window





# Updating .qsf File

- By default, .qsf not updated automatically when constraint entered
- .qsf updated only when
  - Project is saved or closed (File menu)
  - Assignment Editor is saved or closed
  - Beginning of any processing task (e.g. compilation)
  - Any IP parameter editing tool is launched
  - Changing revisions

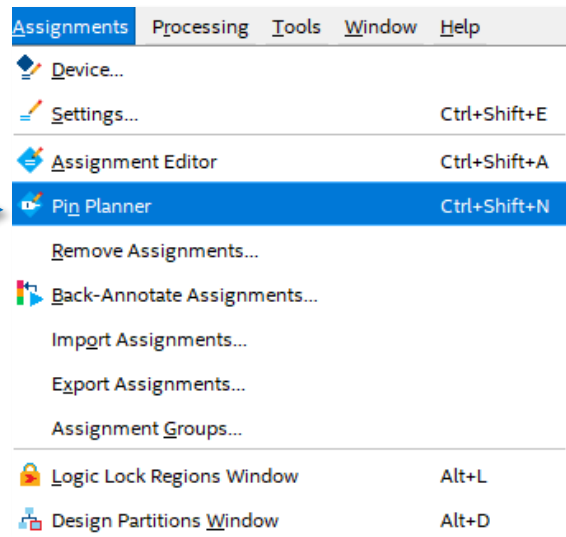


- Change behavior to update assignments immediately (Tools menu → Options → General → Processing)
  - May impact software performance slightly due to file accesses



# I/O assignments

- I/O Planning need
  - I/O standards increasing in complexity
  - FPGA/CPLD I/O structure increasing in complexity
  - PCB development performed simultaneously with FPGA design
  - Pin assignments need to be verified earlier in design cycle
- Creating I/O-Related Assignments
  - **Pin Planner**
  - Import from spreadsheet in **.csv** format
  - Type directly into **.qsf** file
  - Directly in HDL code
  - Scripting





# Pin Planner

Digital Logic Design with FPGA

The screenshot shows the Intel Pin Planner interface for a MAX 10-10M50DAF484C6GES package. The main window displays a top view of the package with pins assigned to various components. A blue box labeled "Groups/Raport View" is overlaid on the left side of the package view. Another blue box labeled "Package View" is overlaid on the right side of the package view. A third blue box labeled "Tasks Pane" is overlaid on the left side of the package view. A fourth blue box labeled "All Pins list" is overlaid on the bottom right of the package view, pointing to the pin list table.

**Pin Legend**

- User I/O
- User assigned I/...
- Filter assigned L...
- Unbonded pad
- Reserved pin
- Other ...
- DEV\_OE
- DEV\_CLR
- DIFF\_n
- DIFF\_p
- DQ
- DQS
- DQSB
- CLK\_n
- CLK\_p
- Other PLL
- Other dual ...
- TDI
- TCK
- TMS
- TDO

**Pin List Table**

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservati
HEX3[4]	Unknown	PIN_C20	6	B6_NO	3.3-V LVTTTL		8mA (default)			
HEX3[5]	Unknown	PIN_D19	6	B6_NO	3.3-V LVTTTL		8mA (default)			
HEX3[6]	Unknown	PIN_E17	6	B6_NO	3.3-V LVTTTL		8mA (default)			
HEX3[7]	Unknown	PIN_D22	6	B6_NO	3.3-V LVTTTL		8mA (default)			
HEX4[0]	Unknown	PIN_F18	6	B6_NO	3.3-V LVTTTL		8mA (default)			
HEX4[1]	Unknown	PIN_E20	6	B6_NO	3.3-V LVTTTL		8mA (default)			
HEX4[2]	Unknown	PIN_E19	6	B6_NO	3.3-V LVTTTL		8mA (default)			
HEX4[3]	Unknown	PIN_J18	6	B6_NO	3.3-V LVTTTL		8mA (default)			



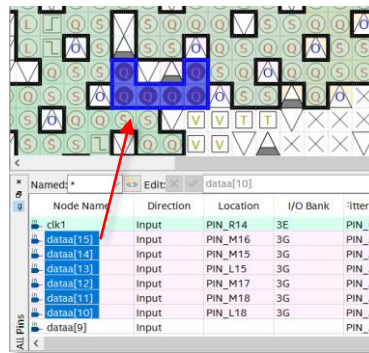
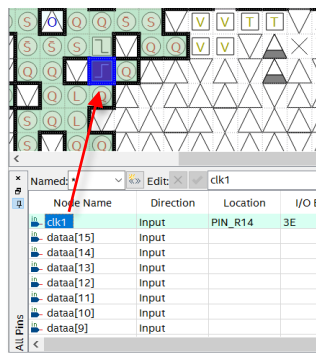
# Pin Planner

- Package View
  - Displays graphical representation of chip package
  - Locate, make, or edit I/O assignments
- All Pins list
  - Displays I/O pins (signals) in design
  - Edit pin assignments
- Groups list
  - Similar to All Pins list displaying only groups & buses
  - Make bus and group assignments
  - Create new user-defined groups
- Tasks pane
  - Perform tasks such as Early Pin Planning and pin highlight reports
- Report Pane
  - Quickly enable/disable reports generated in the Tasks pane



# Pin Planner

- Assigning Pin Locations
  - Drag & drop single top-level I/O signal/pin
  - Drag & drop multiple highlighted pins or buses



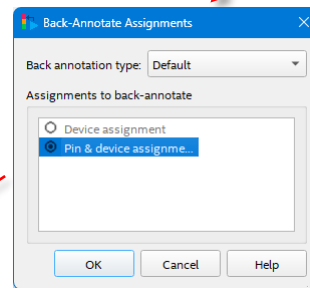
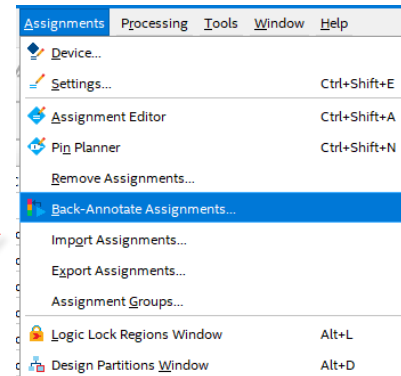
- Select available locations from list of pins color-coded by I/O bank

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate
HEX3[4]	Unknown	PIN_C20	6	B6_NO	3.3-V LVTTTL		8mA (default)	
HEX3[5]	Unknown	PIN_D19						
HEX3[6]	Unknown	PIN_D19	IOBANK_6	Row I/O	DIFFIO_RX_R56n, DIFFOUT_R56n, High_Speed			
HEX3[7]	Unknown	PIN_D21	IOBANK_6	Row I/O	VREFB6N0, High_Speed			
HEX4[0]	Unknown	PIN_E1	IOBANK_1B	Row I/O	DIFFIO_RX_L21n, DIFFOUT_L21n, Low_Speed			
HEX4[1]	Unknown	PIN_E3	IOBANK_1A	Row I/O	ADC2IN8, DIFFIO_RX_L2p, DIFFOUT_L2p, Low_Speed			
HEX4[2]	Unknown	PIN_E4	IOBANK_1A	Row I/O	ADC2IN1, DIFFIO_RX_L2n, DIFFOUT_L2n, Low_Speed			
HEX4[3]	Unknown	PIN_E6	IOBANK_8	Column I/O	PLL_T_CLKOUTn, DIFFIO_RX_T52n, DIFFOUT_T52n, Low_Speed			
		PIN_E8	IOBANK_8	Column I/O	DIFFIO_RX_T48p, DIFFOUT_T48p, Low_Speed			
		PIN_E9	IOBANK_8	Column I/O	DIFFIO_RX_T44n, DIFFOUT_T44n, Low_Speed			
		PIN_E10	IOBANK_8	Column I/O	CLK4n, DIFFIO_RX_T38n, DIFFOUT_T38n, Low_Speed			
		PIN_E11	IOBANK_8	Column I/O	CLK4p, DIFFIO_RX_T38p, DIFFOUT_T38p, Low_Speed			

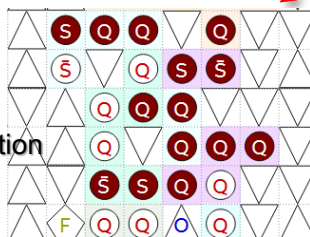


# Pin Planner

- Back-Annotation
  - Use to lock Fitter-chosen pin assignments for future compilations
    - Copies device & resource locations chosen by fitter into .qsf file
      - Pins
      - Logic
    - Routing
  - “Locks down” locations in Pin Planner



Green/brown pattern indicates back-annotation



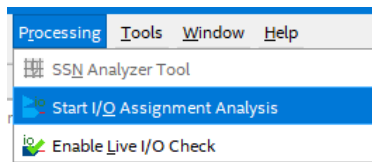




# Pin Planner

## Verifying I/O Assignments

- I/O Assignment Analysis
  - Checks legality of all I/O assignments without full compilation
- Minimal requirements for running
  - I/O declaration
    - HDL port declaration
    - Reserved pin
  - Pin-related assignments
    - I/O standard
    - Current strength
    - Pin location (pin, bank, edge)
    - Toggle rate
- Pin Planner Processing menu → Start I/O Assignment Analysis





# Pin Planner

## I/O Rules Checked

- No internal logic
  - Checks I/O locations & constraints with respect to other I/O & I/O banks
  - e.g. Each I/O bank supports a single VCCIO
- I/O connected to logic
  - Checks I/O locations & constraints with respect to other I/O, I/O banks, & internal resources
  - e.g. PLL must be driven by a dedicated clock input pin
- Note: When working with design files, **synthesize design before running** I/O Assignment Analysis



# I/O Assignment Analysis Output

Messages on I/O assignment issues

- Compiler assumptions
- Device & pin migration issues
- I/O bank voltages & standards

Validating I/O Pin-out

- **Completed design**
  - Run full compilation
  - Enable option to Run I/O Assignment Analysis before compilation (Settings dialog box → Compilation Process Settings)
- **Incomplete design with completed top-level design file**
  - Add I/O-related IP cores and instantiate, even if final connections are not complete
  - Run I/O Assignment Analysis on design

The screenshot shows the I/O Assignment Editor interface. The 'Table of Contents' pane on the left lists various sections, with 'Output Pins' highlighted in blue. A dashed blue box highlights the 'Resource Section' and 'I/O Standards Section' areas. The 'Output Pins' table on the right displays the following data:

	Name	Pin #	I/O Bank
1	hex0[0]	C14	7
2	hex0[1]	E15	7
3	hex0[2]	C15	7
4	hex0[3]	C16	7
5	hex0[4]	E16	7
6	hex0[5]	D17	7
7	hex0[6]	C17	7
8	hex0[7]	D15	7
9	hex1[0]	C18	7
10	hex1[1]	D18	6
11	hex1[2]	E18	6
12	hex1[3]	B16	7
13	hex1[4]	A17	7
14	hex1[5]	A18	7
15	hex1[6]	B17	7
16	hex1[7]	A16	7
17	hex2[0]	B20	6
18	hex2[1]	A20	7
19	hex2[2]	B19	7
20	hex2[3]	A21	6
21	hex2[4]	B21	6
22	hex2[5]	C22	6
23	hex2[6]	B22	6
24	hex2[7]	A19	7
25	hex3[0]	F21	6
26	hex3[1]	E22	6
27	hex3[2]	F22	6

