



Digital Logic  
Design with FPGA

# Design Flow with Quartus

Timing & Power Analysis



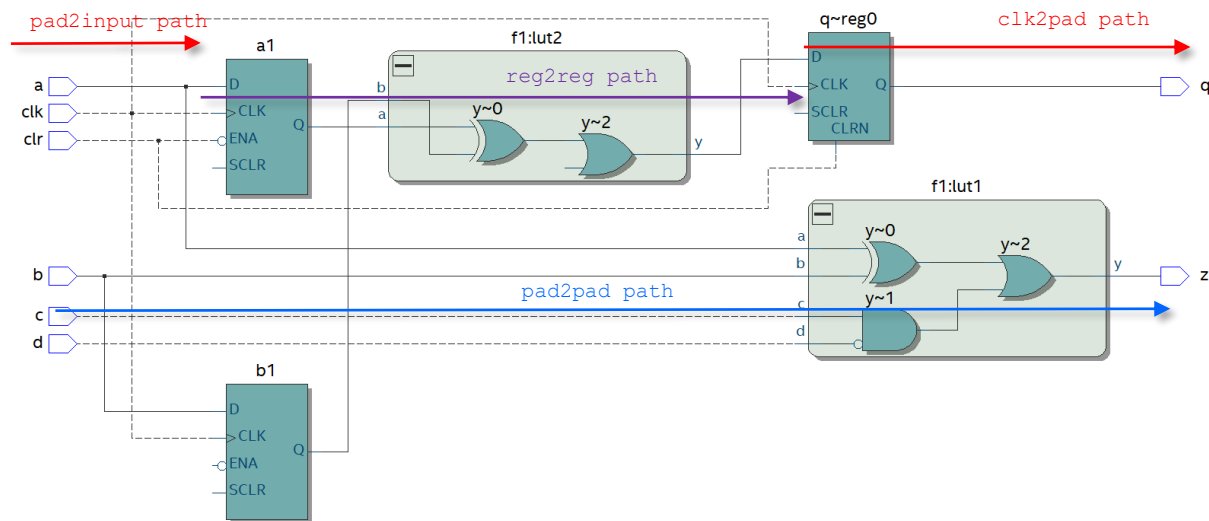
# Outline

- Purpose of timing analysis
- Synchronous analysis
- Asynchronous analysis
- Timing Analyzer
- Timing constraints
- Power analysis tools
  - Early Power Estimations
  - Power Analyzer



# Purpose of Timing Analysis

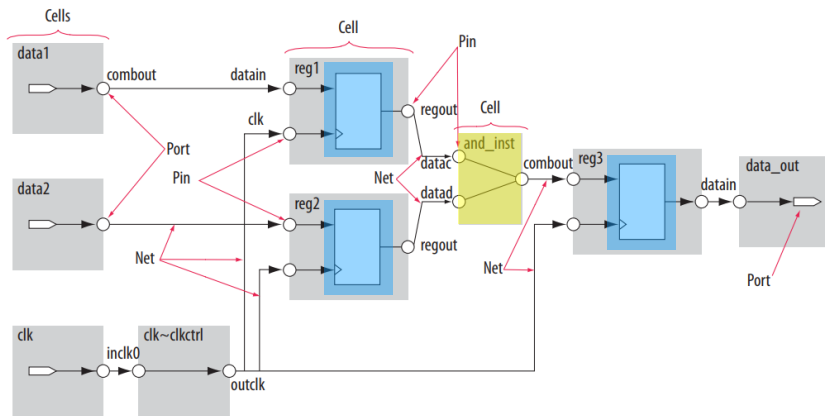
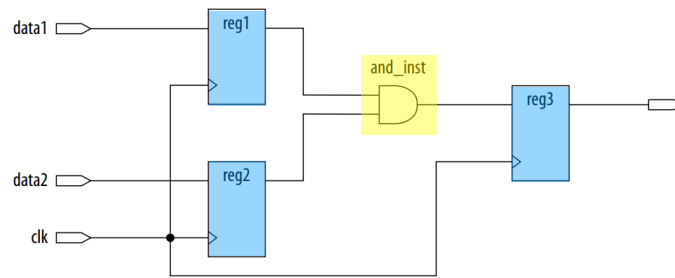
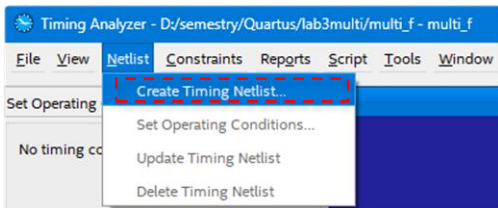
- To analyze design paths against required performance
- Catch timing-related errors faster and easier than gate-level simulation or board testing
- Designer must enter timing expectations
  - Used to guide Fitter during place & route task
  - Used to compare against actual results (post-fit)





# Timing Netlist

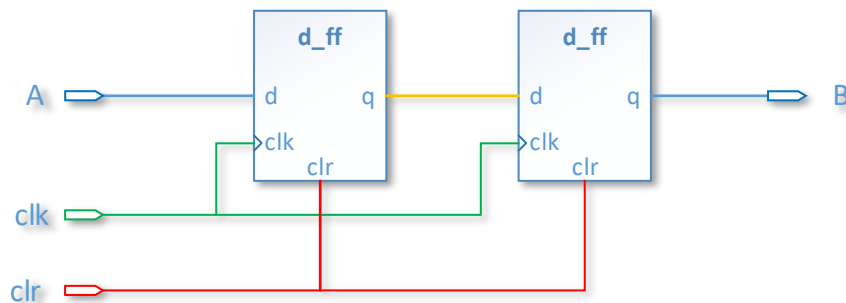
- The Timing Analyzer uses the timing netlist data to determine the data and clock arrival time versus required time for all timing paths
- The timing netlist is generated in the Timing Analyzer any time after running the Fitter or full compilation





# Timing Paths

- Timing paths connect two design nodes, such as the output of a register to the input of another register
  - **Clock paths**—connections from device ports or internally generated clock pins to the clock pin of a register
  - **Data paths**—connections from a port or the data output pin of a sequential element to a port or the data input pin of another sequential element
  - **Asynchronous paths**—connections from a port or asynchronous pins of another sequential element such as an asynchronous reset or asynchronous clear



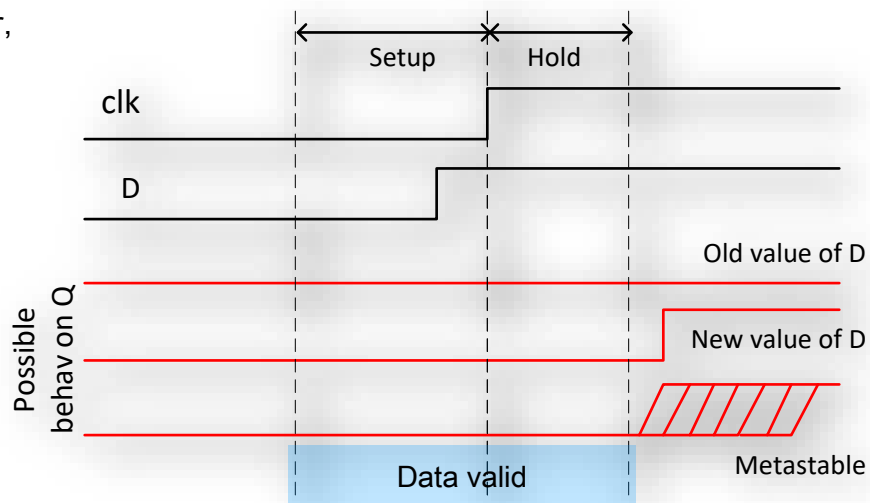
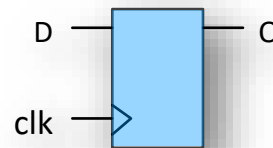
- Types of analysis:
  - Synchronous: clock & data paths
  - Asynchronous: clock & async paths



# Synchronous Analysis

- Check if:
  - Clock and synchronous signals do not arrive at register input at the same time
  - Register output does not become metastable
  - Register transfer data in a known or guaranteed behavior
- Target timing parameters checked
  - Setup time ( $t_{su}$ )
  - Hold time ( $t_h$ )

When you **violate the setup or hold time** of a register, you might oscillate the output, or set the output to an intermediate voltage level between the high and low levels called a **metastable state**





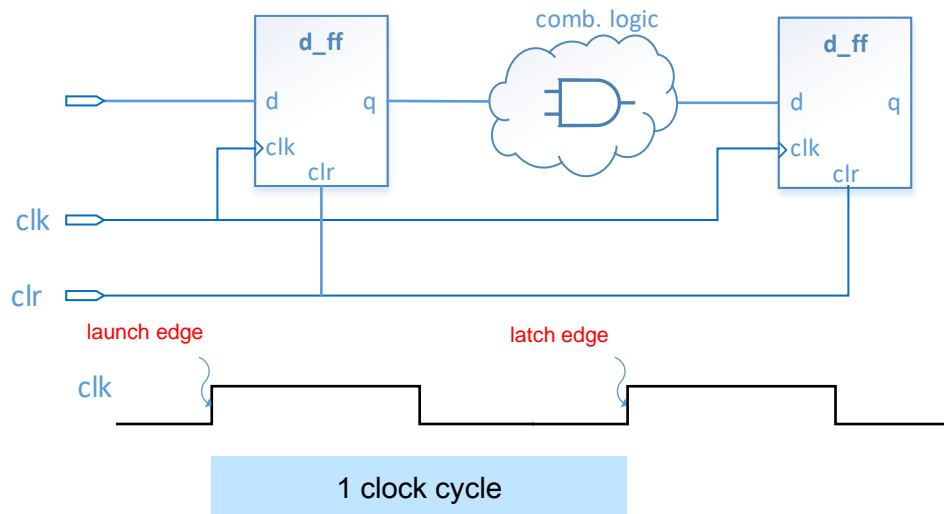
# Synchronous Analysis

Launch edge:

- The edge which “launches” the data from the source register

Latch edge:

- The edge which “latches” the data at the destination register (with respect to the launch edge, selected by timing analyzer, typically 1 clock cycle, i.e. rising to rising edge)

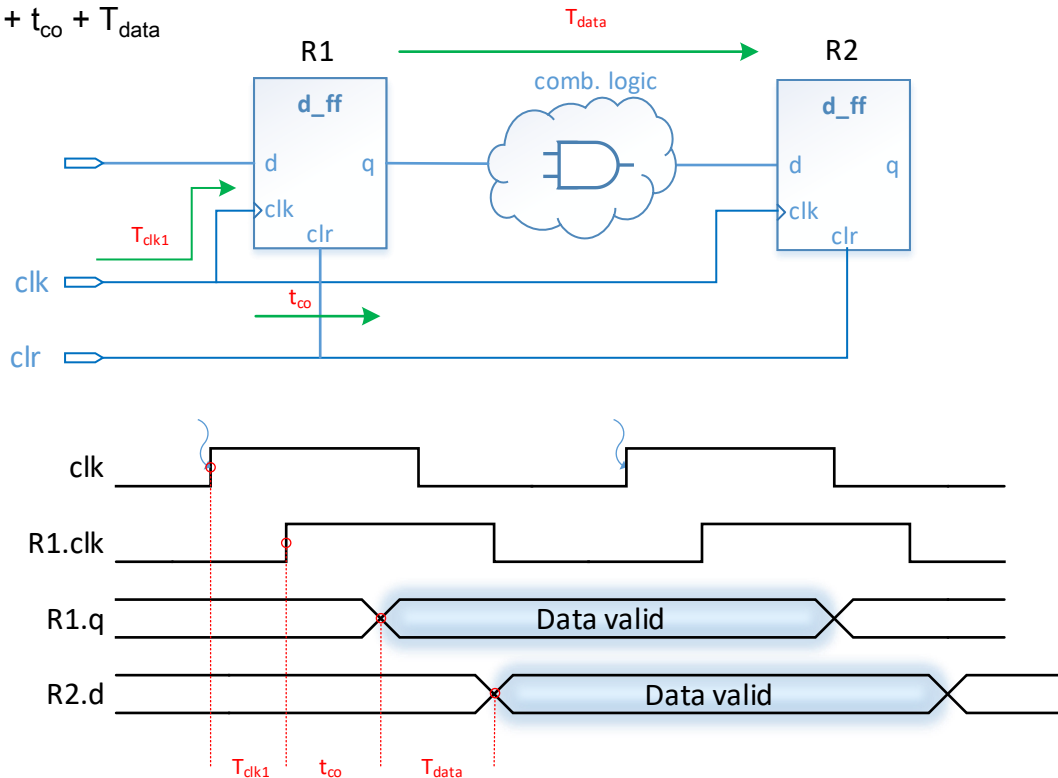




# Synchronous Analysis

Data arrival time:

- The time for data to arrive at the destination register's D input
- Data arrival time = launch edge +  $T_{clk1}$  +  $t_{co}$  +  $T_{data}$



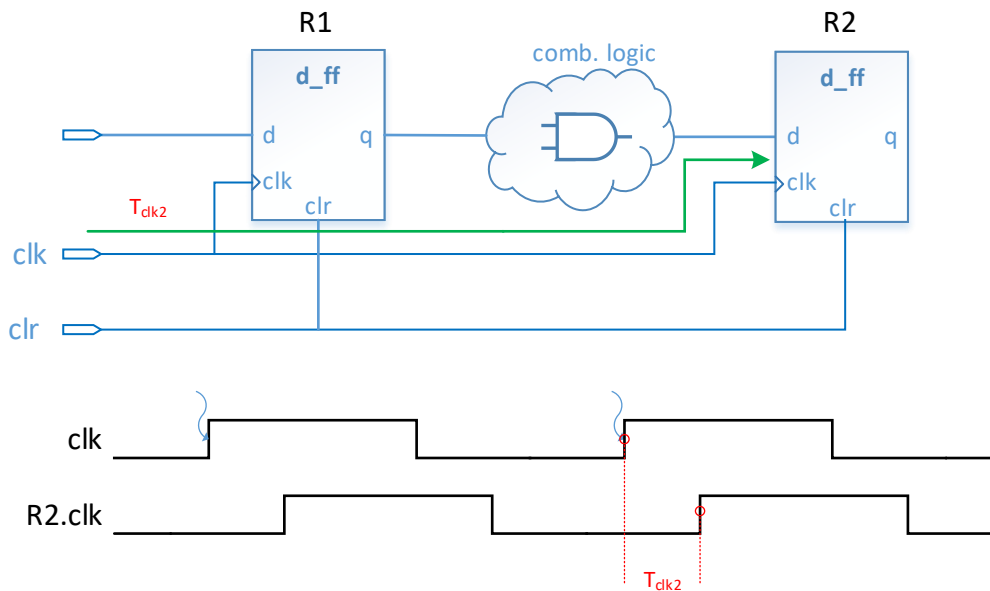




# Synchronous Analysis

Clock arrival time:

- The time for clock to arrive at the destination register's clock input
- Clock arrival time = latch edge +  $T_{clk2}$

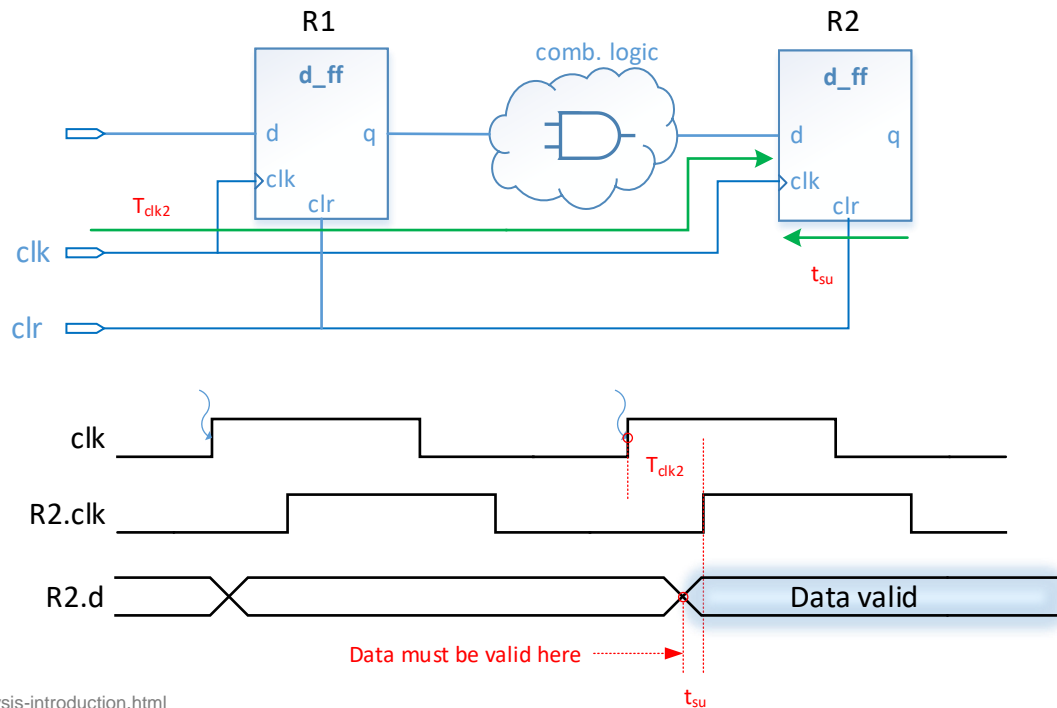




# Synchronous Analysis

Data required time (Setup):

- The minimum time required for data to be valid before the latch edge (the data can be successfully latched into destination register R2)
- Data required time (Setup) = (latch edge +  $T_{clk2}$ ) -  $t_{su}$  - Setup uncertainty

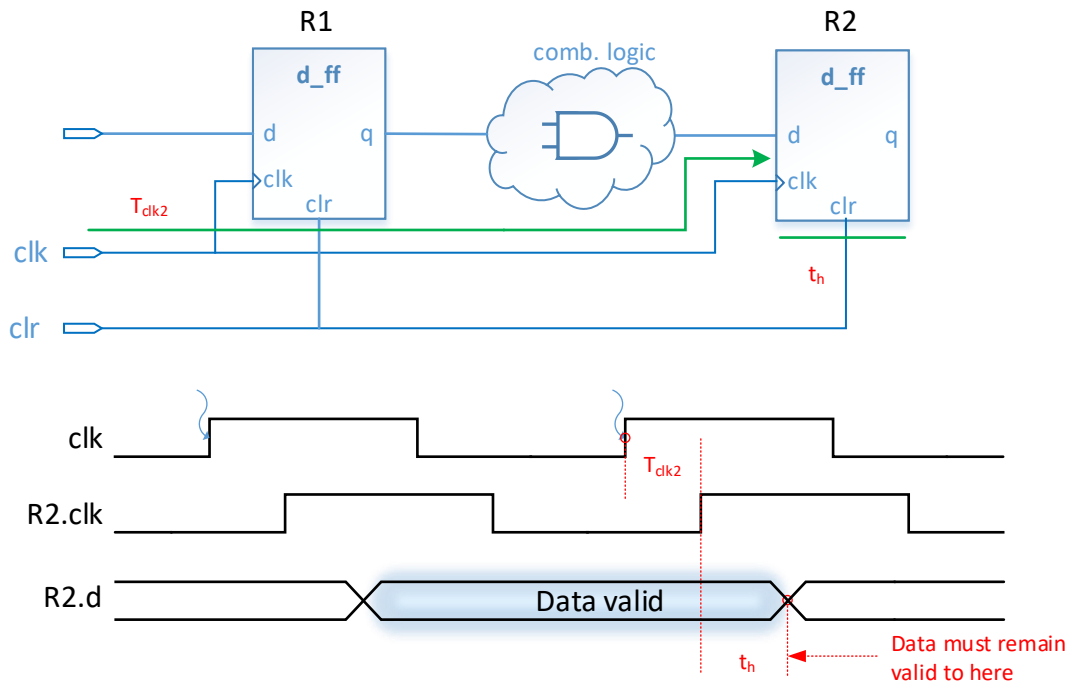




# Synchronous Analysis

Data required time (Hold):

- The minimum time required after the latch edge for data to remain valid (the data can be successfully latched into destination register R2)
- Data required time (Hold) = (latch edge +  $T_{clk2}$ ) +  $t_h$  + Hold uncertainty





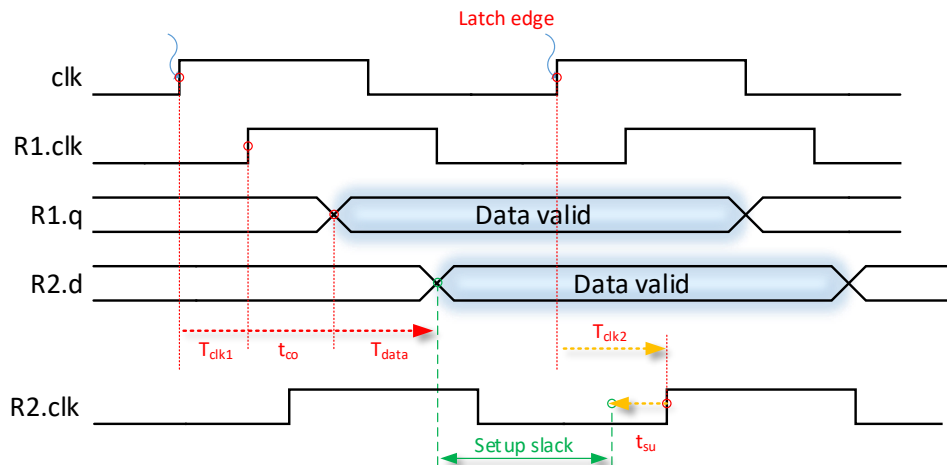
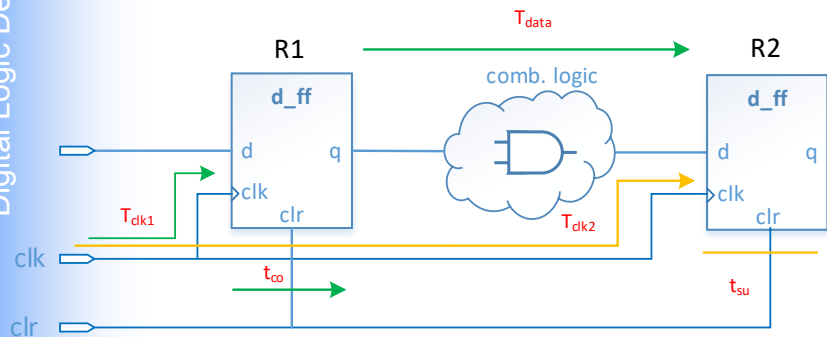
# Synchronous Analysis

Calculating Setup Slack:

- Margin by which the **setup timing requirement** is met
- Ensures launched data arrives in time to meet the latching requirement

Setup slack = Min. Data Required Time (Setup) – Max. Data Arrival Time

- Positive slack – timing requirement met
- Negative slack – timing requirement not met





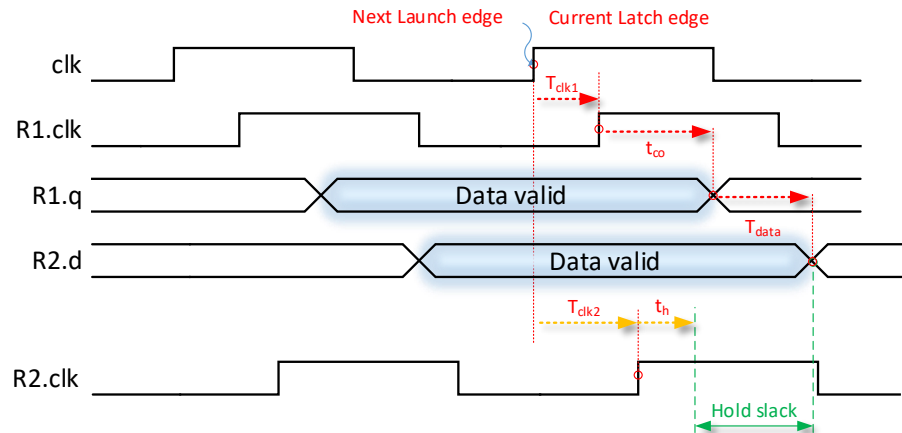
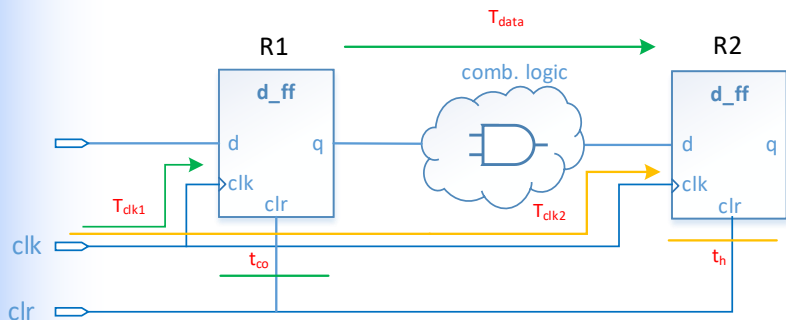
# Synchronous Analysis

Calculating Hold Slack:

- Margin by which the hold timing requirement is met
- Ensures latched data is not corrupted by data from the next launch edge (the input data cannot change too quickly after rising edge of the clock)

Hold slack = Min. Data Arrival Time – Max. Data Required Time (Hold)

- Positive slack – timing requirement met
- Negative slack – timing requirement not met

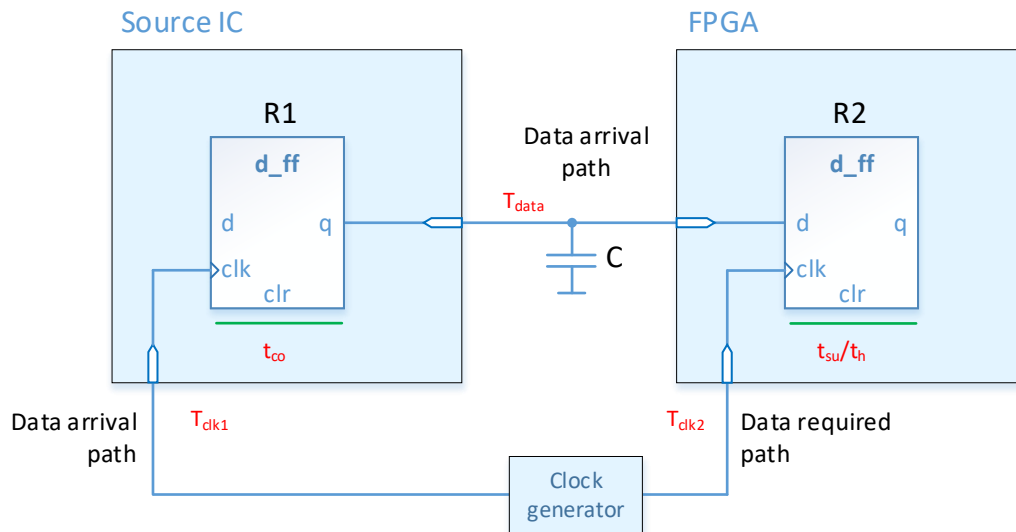




# Synchronous Analysis

I/O Analysis (Common Clock Source):

- Analyze I/O performance in a synchronous design using the same slack equations from the prior slides
- Must include external device & printed circuit board timing parameters



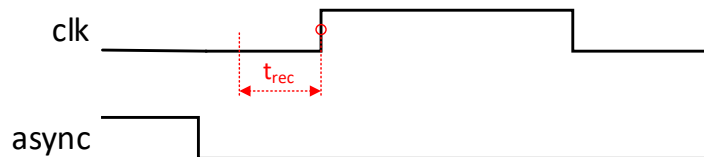


# Asynchronous Analysis

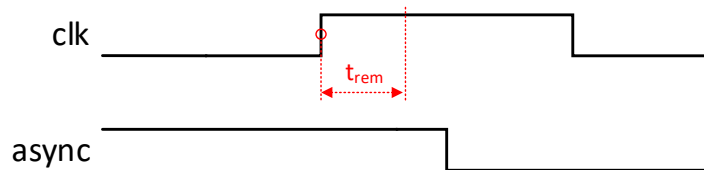
- Check if:
  - Clock and asynchronous signals (i.e. clear) do not arrive at register input at the same time
  - Register output does not become unstable
  - Registers come out of asynchronous condition at the same time and in a known state

- Target timing parameters checked

- **Recovery** time ( $t_{rec}$ )  
minimum time an asynchronous signal must be de-asserted **before** clock edge



- **Removal** time ( $t_{rem}$ )  
minimum time an asynchronous signal must be de-asserted **after** clock edge





# Asynchronous Analysis

Recovery slack = Min. Required Time (Recovery) – Max. Arrival Time

Removal slack = Min. Arrival Time – Max. Required Time (Removal)

- Positive slack – timing requirement met
- Negative slack – timing requirement not met





# Timing Models

Intel Quartus Prime models device timing at multiple process voltage temperature (PVT)

- **Slow corner** model
  - Indicates slowest possible performance for any single path
  - Timing for slowest device at maximum operating temperature and lowest voltage (VCCMIN)
- **Fast corner** model
  - Indicates fastest possible performance for any single path
  - Timing for fastest device at minimum operating temperature and highest voltage (VCCMAX)
- **2<sup>nd</sup> slow** and **2<sup>nd</sup> fast** models
  - Slow timing at minimum operating temperature
  - Fast timing at maximum operating temperature
  
- ! Ensure **setup timing is met in the slow models**
- ! Ensure **hold timing is met in fast model** (essential for source synchronous interface)



# Timing Analyzer GUI

- Timing analysis engine in Quartus Prime providing timing analysis solution for all level of experience
- Features:
  - Synopsys Design Constraints (SDC) support
  - Easy-to-use interface
    - Graphical constraint entry
    - Standard, on-the-fly reporting
  - Scripting fully supported

The screenshot displays the Timing Analyzer interface for a design named 'filter - filter\_w\_pll'. The main window shows a table of setup paths with the following data:

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay	Worst-Case
0.813	inst3[result[1]]	yn_out[7]-reg0	clk_250	clk_500	2.000	-0.301	0.900	Slow 900mV
1.054	inst3[result[8]]	yn_out[4]-reg0	clk_250	clk_500	2.000	-0.279	0.713	1 Slow vid1
1.063	inst3[result[9]]	yn_out[5]-reg0	clk_250	clk_500	2.000	-0.291	0.646	1 Slow vid1
1.137	inst3[result[4]]	yn_out[0]-reg0	clk_250	clk_500	2.000	-0.277	0.587	1 Slow vid1
1.146	inst3[result[5]]	yn_out[1]-reg0	clk_250	clk_500	2.000	-0.284	0.573	1 Slow vid1

The interface also includes a 'Report' section with a tree view showing 'Timing Delays: Final Snapshot', 'Advanced I/O Timing', 'SDC File List', 'Setup Summary', and 'Setup: clk\_500'. A 'Tasks' panel lists actions like 'Open Project...', 'Create Timing Netlist', 'Read SDC File', 'Update Timing Netlist', 'Reset Design', 'Set Operating Conditions...', 'Reports', and 'Slack'. A waveform diagram on the right shows the timing relationship between the Launch Clock, Latch Clock, Setup Relationship, Data Arrival, and Clock Delay, with a total setup slack of -0.872 ns. The console window at the bottom displays the following TAP script:

```
1 Automatically reporting setup summary. To change this behavior, see Timer Analyzer Settings.
2 tdi report_timing -to_clock { clk_500 } -setup -npaths 10 -extra_info none -detail full_path -panel_name {Setup: clk_500}
3 tdo Report Timing: Found 8 setup paths (0 violated). worst case slack is 0.813
4 tcl 8 0.813
```



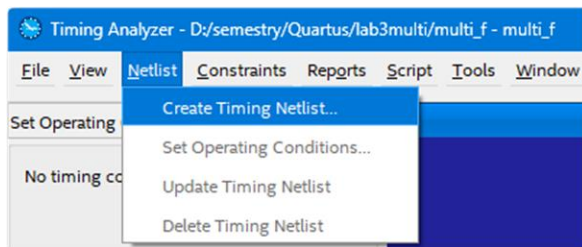
# Timing Constraints

## Constraining recommendations

- Ensure all design path are constrained
  - Constraints guide the Fitter during placement & routing design
  - Without guidance, Fitter can make incorrect optimization choice
  - Design paths must be constrained to fully analyze design
  - Timing Analyzer only performs slack analysis on constrained paths

## Basis timing analysis flow

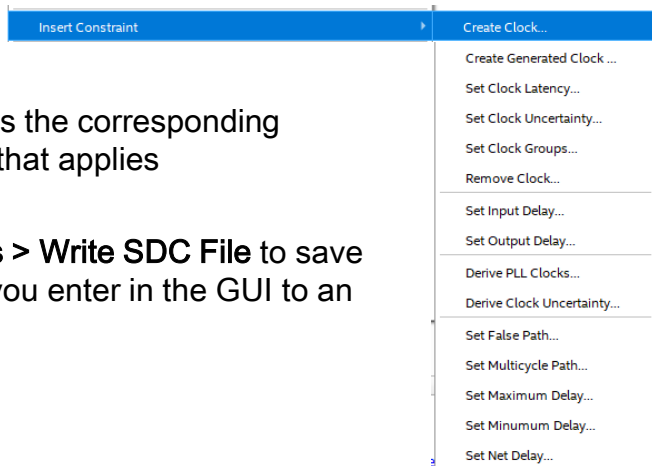
- Create a Project and run the Fitter
- Create Timing Netlist
- Specify timing constraints
- Run timing analysis
- Analyze results



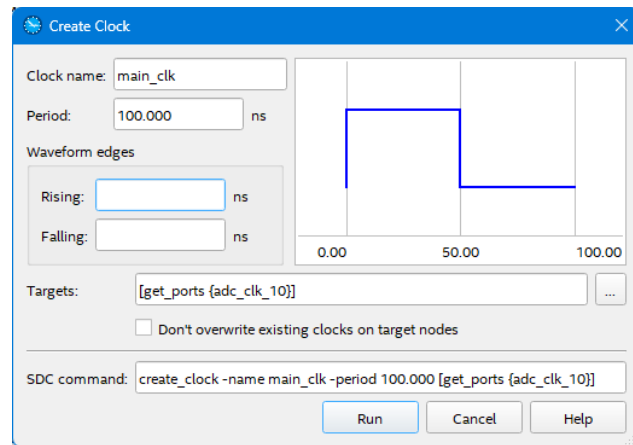


# Timing Analyzer GUI

- Enter constraints in the Timing Analyzer GUI
  - Create clock constraint



- The GUI displays the corresponding SDC command that applies
- click **Constraints > Write SDC File** to save the constraints you enter in the GUI to an **.sdc** file

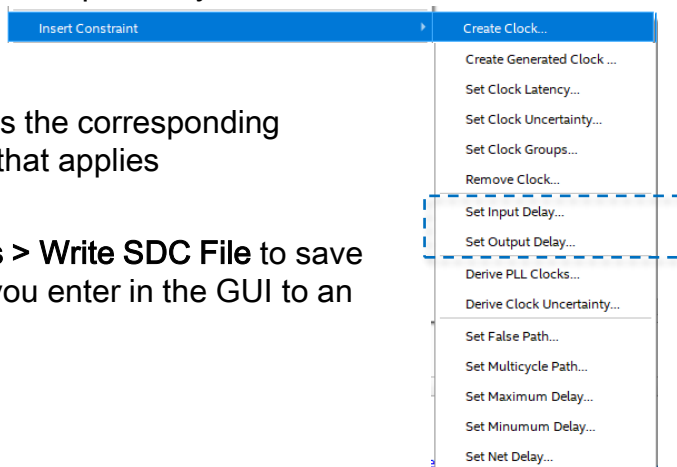


```
create_clock -name {main_clk} -period 100.000 -waveform { 0.000 50.000 } [get_ports {adc_clk_10}]
```

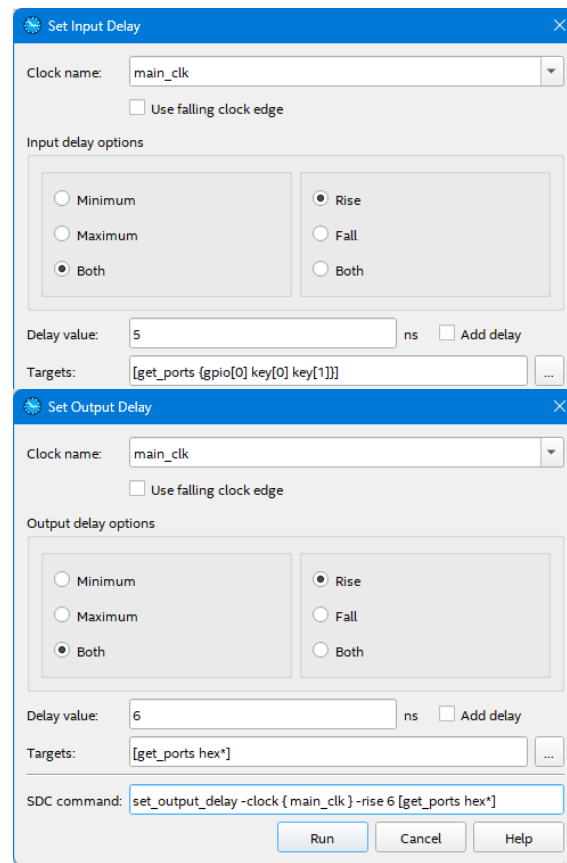


# Timing Analyzer GUI

- Enter constraints in the Timing Analyzer GUI
  - Create input/output delay constraints



- The GUI displays the corresponding SDC command that applies
- click **Constraints > Write SDC File** to save the constraints you enter in the GUI to an **.sdc** file



```
set_input_delay -clock { main_clk } -rise 5 [get_ports {gpio[0] key[0] key[1]}]
set_output_delay -clock { main_clk } -rise 6 [get_ports hex*]
```



# Timing Analyzer GUI

## Analysis of time results

Digital Logic Design with FPGA

Multi Corner Summary (2/3 corners)

	Corner	Slack	From
951	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
952	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
953	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
954	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
955	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
956	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
957	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
958	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
959	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
960	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
961	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
962	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
963	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
964	Slow 1200mV 85C Model	95.502	sld_sigaltap:auto_sigaltap_0 sld_sigaltap...
965	Slow 1200mV 85C Model	95.507	sld_hub:auto_hub alt_sld_fab_with_jtag_input
966	Slow 1200mV 85C Model	95.509	sld_hub:auto_hub alt_sld_fab_with_jtag_input
967	Slow 1200mV 85C Model	95.509	sld_hub:auto_hub alt_sld_fab_with_jtag_input
968	Slow 1200mV 85C Model	95.509	sld_hub:auto_hub alt_sld_fab_with_jtag_input
969	Slow 1200mV 85C Model	95.509	sld_hub:auto_hub alt_sld_fab_with_jtag_input
970	Slow 1200mV 85C Model	95.509	sld_hub:auto_hub alt_sld_fab_with_jtag_input
971	Slow 1200mV 85C Model	95.514	sld_hub:auto_hub alt_sld_fab_with_itae_input

The screenshot shows the Timing Analyzer GUI with the following components:

- Set Operating Conditions:** Fast 1200mV 0C Model selected.
- Report:** All Clock Histograms > Slow 1200mV 85C Model > main\_clk (Setup).
- Tasks:** Report Top Failing Paths, Report All I/O Timings, Report All Core Timings.
- Bar Chart:** Shows Edges (Y-axis, 0-900) vs Slack (X-axis, 84.843 ns to 99.363 ns). The distribution shows a peak at approximately 95.5 ns.
- Console:** Contains the following command:
 

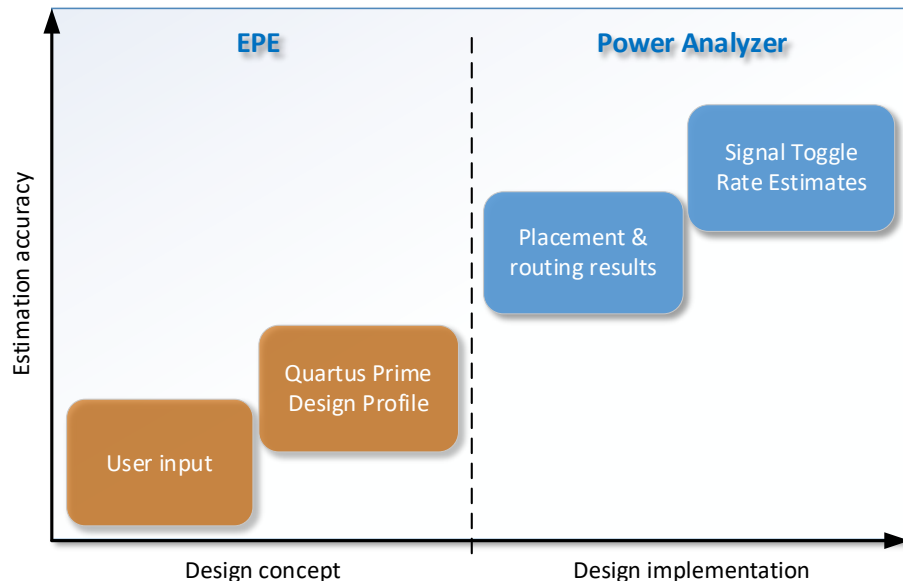
```
report_datasheet -multi_corner -panel_name {Datasheet Report}
report_rskm -multi_corner -panel_name RSKM
report_ddr -multi_corner -panel_name DDR
report_metastability -multi_corner -panel_name {Summary (Metastability)}
create_slack_histogram -multi_corner -panel_name {Slack Histogram (main_clk)} -clock_name [get_clocks {main_clk}] -num_bins 20
create_timing_summary -setup -multi_corner -panel_name {Summary (Setup)}
create_timing_summary -hold -multi_corner -panel_name {Summary (Hold)}
create_timing_summary -recovery -multi_corner -panel_name {Summary (Recovery)}
create_timing_summary -removal -multi_corner -panel_name {Summary (Removal)}
create_timing_summary -mpw -multi_corner -panel_name {Summary (Minimum Pulse Width)}
report_max_skew -multi_corner -panel_name {Summary (Max Skew)} -detail summary
report_net_delay -multi_corner -panel_name {Summary (Net Delay)} -nworst 0
create_slack_histogram -multi_corner -panel_name {All Clock Histograms} -clock_name [get_clocks *] -num_bins 30
set_operating_conditions "MIN_fast_1200mv_0c"
```



# Power Analysis Tools

Quartus Prime provides tools to estimate power consumption in a FPGA design at different stages of the design process

- **Early Power Estimator (EPE)** to estimate the power consumption before compilation
  - Reliable estimate before design development
  - Spreadsheet-based “what-if” analysis
- **Power Analyzer** to estimate power consumption for a post-fit design
  - Detailed design power estimation
  - Use actual design place & route and logic configuration
  - High accuracy





# Early Power Estimator

- For quick “what-if” analysis
- Enter design data manually before design
- Generate design inputs in Quartus Prime for more accurate analysis (<=>\_early\_power.csv)

## Input:

- Number of registers
- Transition rates
- Clocks and frequency
- IO and memory
- DSP and PLL
- Temperature, air flow, heat sinking

Visit the Online Power Management Resource Center

PowerPlay Early Power Estimator Max<sup>®</sup> 10

V18.1, Build 09.25

### Input Parameters

Family	MAX 10
Device	10M02DC
Package	U324
Temperature Grade	Commercial
Power Characteristics	Typical
V <sub>CC_ONE</sub> Voltage (V)	N/A
Power Model Status	FINAL

User Entered T<sub>J</sub>  Auto Computed T<sub>J</sub>

Ambient Temp, T<sub>A</sub> (°C) 25

Custom Theta JA  Estimated Theta JA

Heat Sink 23 mm - Medium Profile

Airflow 200 lfm (1.0 m/s)

Custom  $\theta_{sa}$ (°C/W) 6.40

Board Thermal Model None (Conservative)

### Thermal Power (mW)

Logic	0.00
RAM	0.00
DSP	0.00
I/O	0.00
PLL	0.00
Clock	0.00
P <sub>static</sub>	36.41
<b>TOTAL (mW)</b>	<b>36.41</b>

[Intel recommends using Intel® Enpirion® Power Solutions with Intel® FPGAs](#)

### Thermal Analysis

Junction Temp, T <sub>J</sub> (°C)	25.8
$\theta_{JA}$ Junction-Ambient	21.80
Maximum Allowed T <sub>J</sub> (°C)	84.1

Details

### Power Tree Design

Power Rail Configuration

N/A		
Regulator	Voltage	Current
Regulator 1	N/A	N/A
Regulator 2	N/A	N/A
Regulator 3	N/A	N/A
Regulator 4	N/A	N/A
Regulator 5	N/A	N/A
Regulator 6	N/A	N/A
Regulator 7	N/A	N/A
Regulator 8	N/A	N/A

Set Toggle % Reset View Report Import CSV Export CSV

Select Power Regulator

Main Logic RAM DSP IO PLL Clock Report Enpirion Release Notes

Download form Intel website

- [https://www.intel.com/content/dam/altera-www/global/en\\_US/others/support/devices/estimator/max-10-estimator/max10\\_epe.xls](https://www.intel.com/content/dam/altera-www/global/en_US/others/support/devices/estimator/max-10-estimator/max10_epe.xls)





# Early Power Estimator

Thermal Power information

PowerPlay Early Power Estimator Max<sup>®</sup> 10  
V18.1, Build 09.25

Visit the Online Power Management Resource Center

### Input Parameters

Family: MAX 10  
Device: 10M02DC  
Package: U324  
Temperature Grade: Commercial  
Power Characteristics: Typical  
V<sub>CC,ONE</sub> Voltage (V): N/A  
Power Model Status: FINAL

User Entered T<sub>j</sub>     Auto Computed T<sub>j</sub>

Ambient Temp, T<sub>A</sub> (°C): 25  
 Custom Theta JA     Estimated Theta JA

Heat Sink: 23 mm - Medium Profile  
Airflow: 200 lfm (1.0 m/s)  
Custom  $\theta_{SA}$ (°C/W): 6.40  
Board Thermal Model: None (Conservative)

### Thermal Power (mW)

Logic	0.00
RAM	0.00
DSP	0.00
I/O	0.00
PLL	0.00
Clock	0.00
P <sub>static</sub>	36.41
<b>TOTAL (mW)</b>	<b>36.41</b>

[Intel recommends using Intel® Enpirion® Power Solutions with Intel® FPGAs](#)

### Thermal Analysis

Junction Temp, T<sub>J</sub> (°C): 25.8  
 $\theta_{JA}$  Junction-Ambient: 21.80  
Maximum Allowed T<sub>A</sub>(°C): 84.1

[Details](#)

### Power Tree Design

Power Rail Configuration: N/A

	Voltage	Current
Regulator 1	N/A	N/A
Regulator 2	N/A	N/A
Regulator 3	N/A	N/A
Regulator 4	N/A	N/A
Regulator 5	N/A	N/A
Regulator 6	N/A	N/A
Regulator 7	N/A	N/A
Regulator 8	N/A	N/A

Set Toggle %    Reset    View Report    Import CSV    Export CSV    Select Power Regulator

Main    Logic    RAM    DSP    IO    PLL    Clock    Report    Enpirion    Release Notes

Input Parameter information

Thermal Analysis information

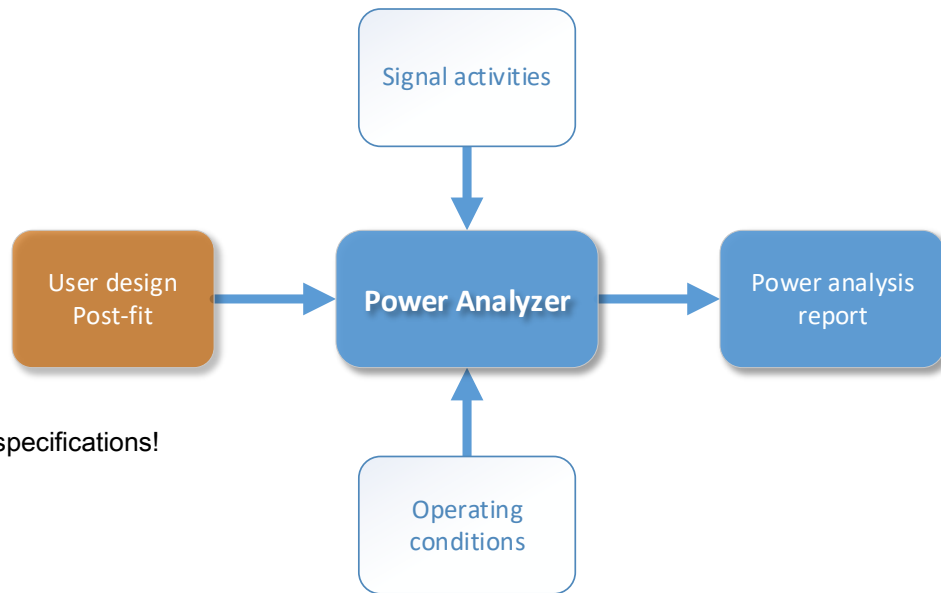
Power Tree Design

Resource information tabs



# Power Analyzer

- Data inputs:
  - Post-fit design
  - Clock requirements
  - Signal activity defaults
  - Environmental conditions
  - Register transfer level (RTL) simulation results (optional)
  - Post-fit simulation results (optional)
  - Signal activities per node or entity (optional)
- Data outputs:
  - Total thermal power
  - Thermal static power
  - Thermal dynamic power
  - Thermal I/O power
  - Thermal power by design hierarchy
  - Thermal power by block type
  - Thermal power dissipation by clock domain
  - Off-chip (non-thermal) power dissipation
  - Device supply currents



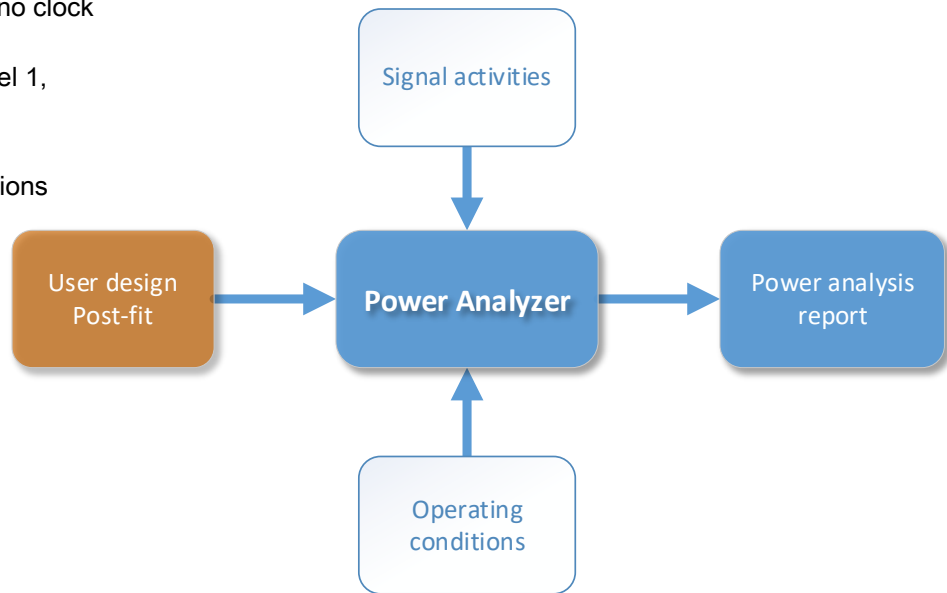
**Note:** Do not use the results of the Power Analyzer as design specifications!



# Power Analyzer

## Signal activity inputs:

- Value change dump file (.vcd)
  - Captures signal toggling information
  - Created by Questa simulator
- Assignments applied to entities in Assignment Editor or script
  - **Power Toggle Rate:**  
absolute toggle rate in transitions/s
  - **Power Toggle Rate Percentage:**  
toggle rate relative to clock driving node; ignore if no clock
  - **Power Static Probability:**  
fraction of analysis time when signal is at logic level 1, ranges between 0 and 1
- Default toggle rate (12,5%)
  - Percentage of clock periods in which signal transitions
  - Absolute number of transitions per second





# Power Analyzer

## Operating conditions

Specifies the device characteristics to be used during power estimation. Estimates are based on average power consumed by typical silicon at nominal operating conditions.

- **Typical** – nominal operating conditions for device
- **Maximum** – worst-case conditions, use for power budgeting and supply design (timing analysis always uses worst-case!)
- **Voltage settings** (options differ depending on device selected)
- **Operating temperature** (package temperature and cooling solution)

The screenshot shows the 'Settings - multi\_f' window with the 'Operating Settings and Conditions' section selected in the left-hand navigation pane. The main content area is divided into three sections: 'Operating Settings and Conditions', 'Voltage', and 'Temperature'.

**Operating Settings and Conditions**

Select the device power characteristics.

Device power characteristics:

SmartVoltage ID:

**Voltage**

Select the operating voltage conditions.

Name:	Setting:
VCCINT voltage	1.2V
VCCA voltage	2.5V
VCCD voltage	1.2V
VCCIO voltage	Configurable through pin assignments

**Temperature**

Select the operating temperature conditions.

Junction temperature range

Minimum temperature:  °C    Maximum temperature:  °C

Junction temperature and cooling solution settings for power analysis

Specify junction temperature:  °C

Auto compute junction temperature using cooling solution

Ambient temperature:  °C

Thermal resistances

Use cooling solution:

Junction-to-case: 4.7°C/W    Case-to-heat sink: °C/W

Case-to-ambient: 18.60°C/W

**Board thermal modeling**

Board thermal model: Included in case-to-ambient-thermal resistance

Junction-to-board: °C/W    Board temperature:  °C



# Power Analyzer

## Running the Analyzer

- **Processing menu -> Power Analyzer Tool**
  - or enable running during full compilation
  - and viewing report

