Custom Computing & Embedded Systems

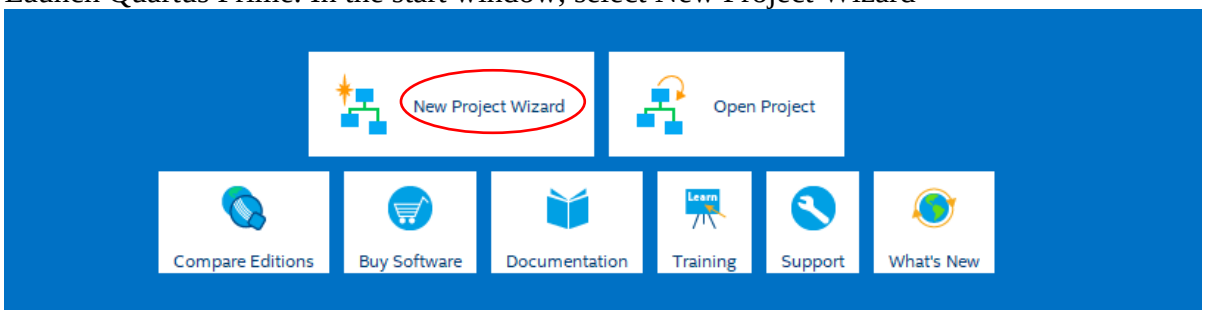
Quartus Prime – simulation

Example of configuring and running the Questa simulator from the Quartus Prime project. Two types of simulations will be performed: RTL and Gate-level.

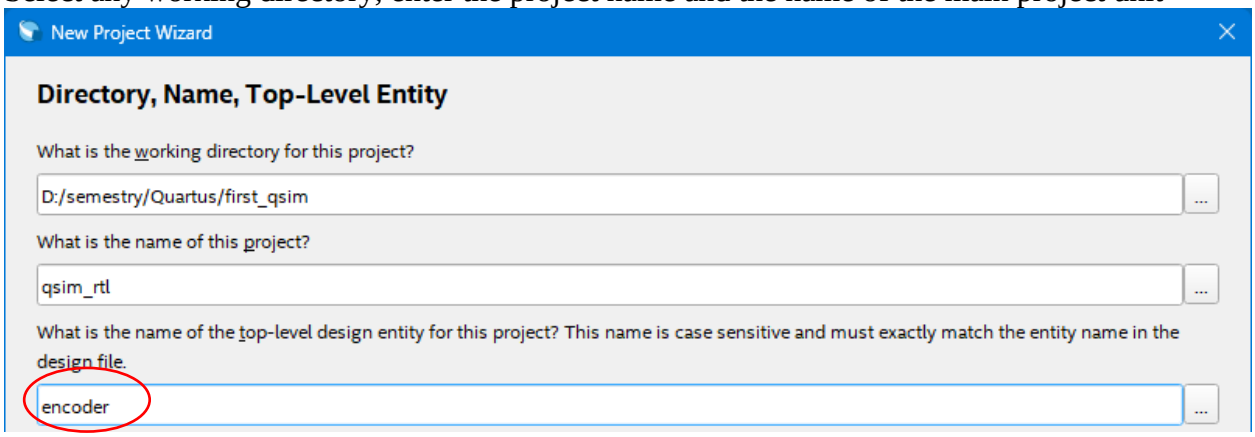
The description of the activities provided assumes the existence of sources for synthesis (**encoder**.vhd) and testbench (**encoder_tb**.vhd).

1. Preparing the project

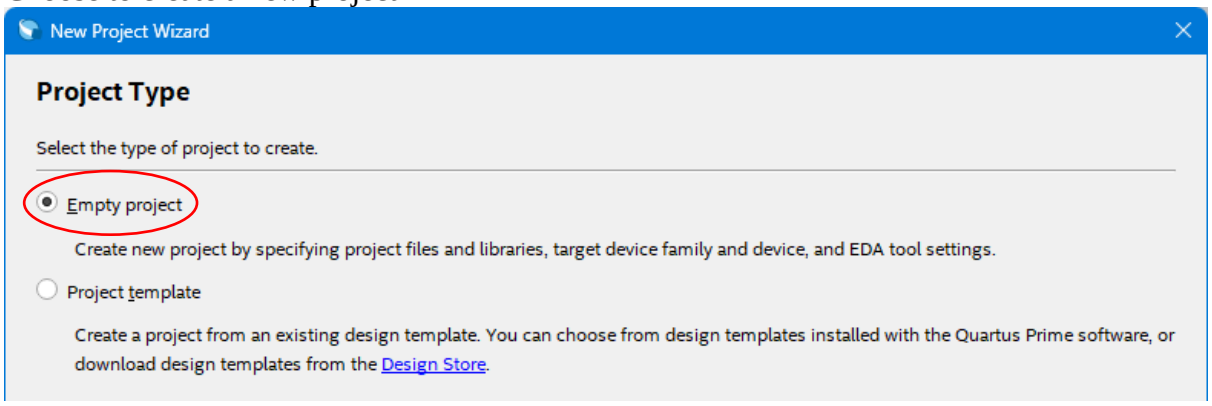
Launch Quartus Prime. In the start window, select New Project Wizard



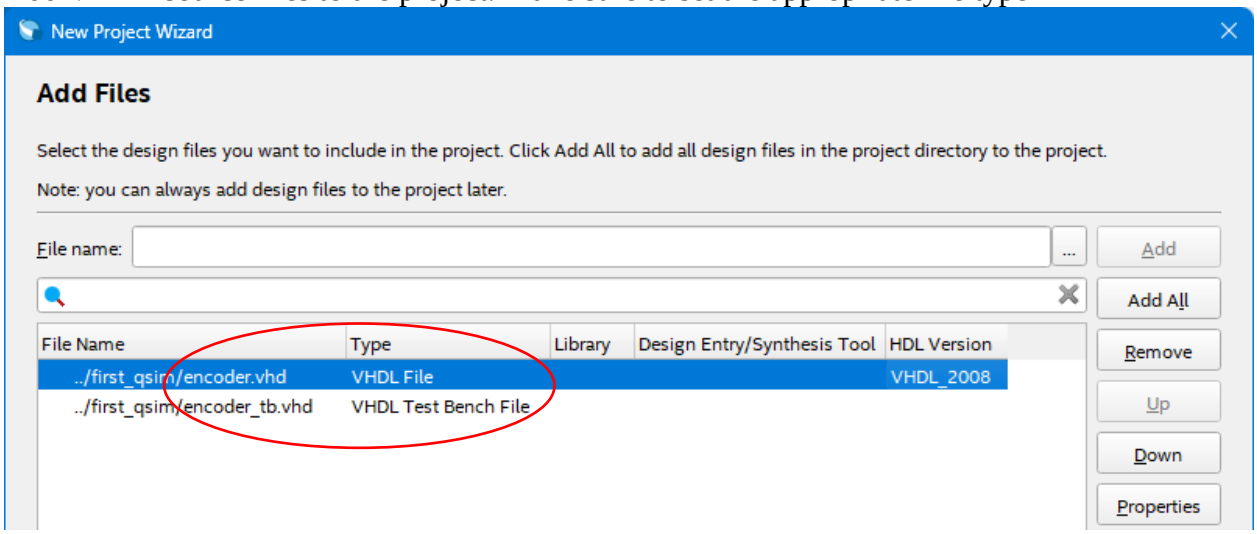
Select any working directory, enter the project name and the name of the main project unit



Choose to create a new project

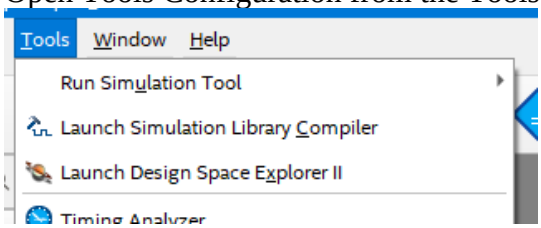


Add VHDL source files to the project. Make sure to set the appropriate file type



2. Configuring EDA tools

Open Tools Configuration from the Tools menu



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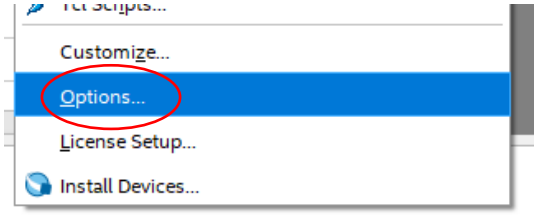
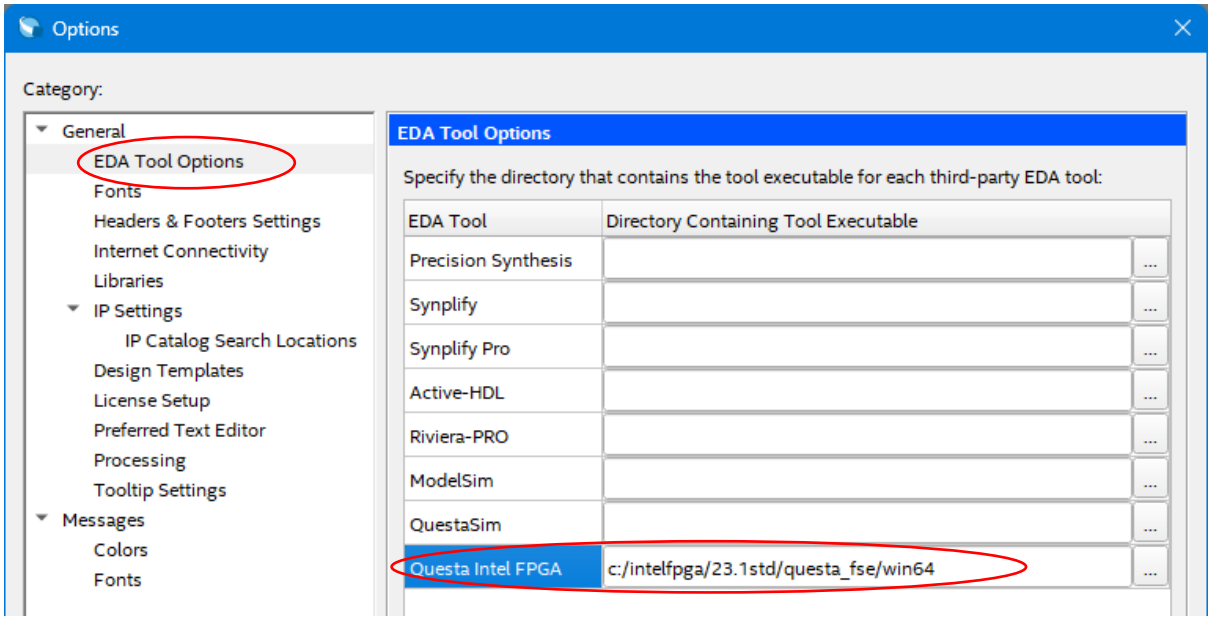
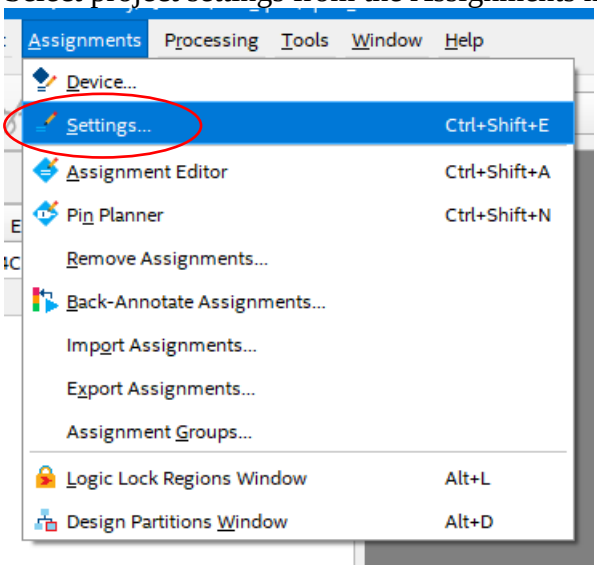


Check the correct settings of the EDA tools, if necessary, set the appropriate path to the Questa simulator

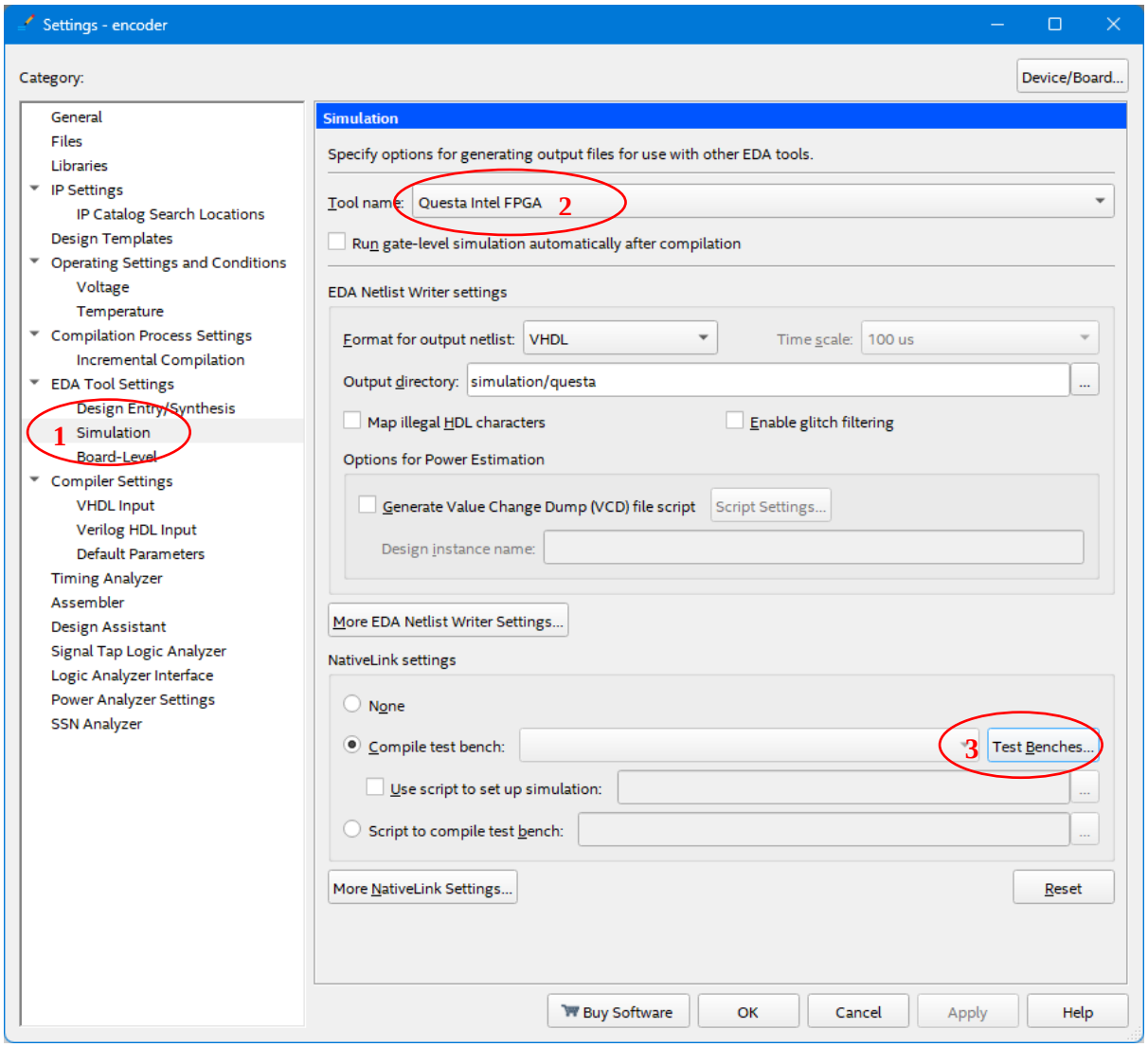


3. Simulation setup

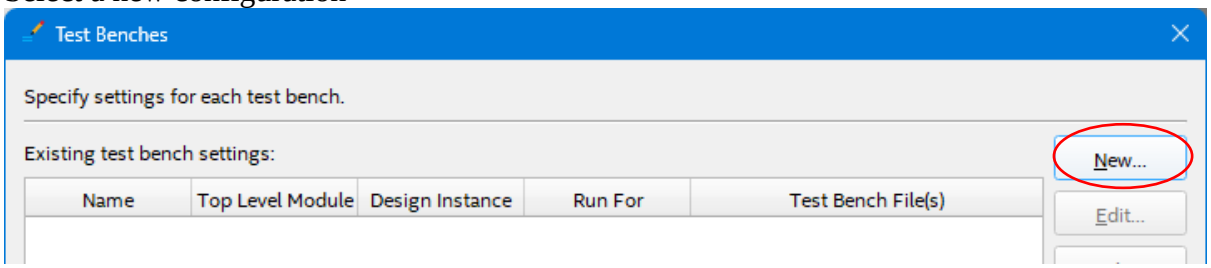
Select project settings from the Assignments menu



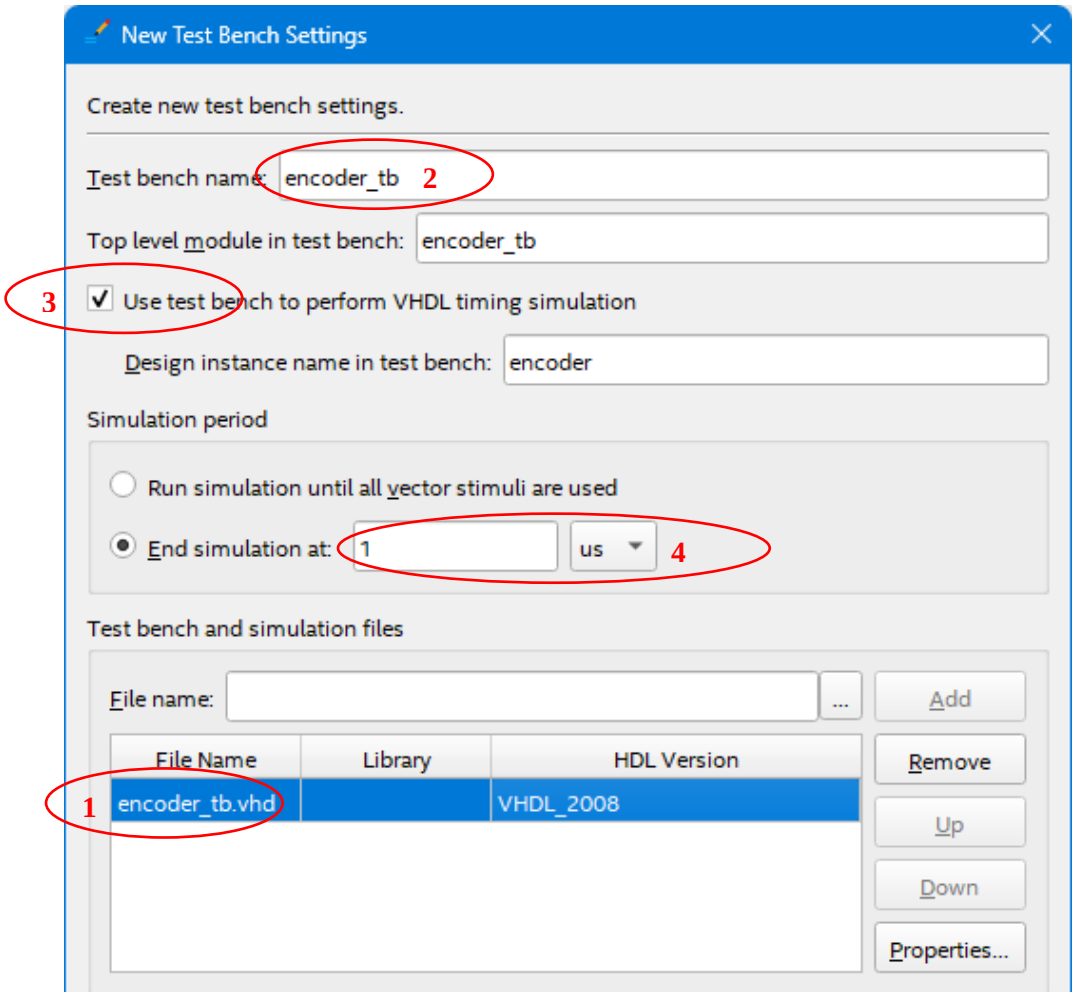
In the settings window, find the simulation parameters (1).
Select the Quest Intel FPGA simulator (2)
and go to the testbench configuration in the NativeLink settings group (3)

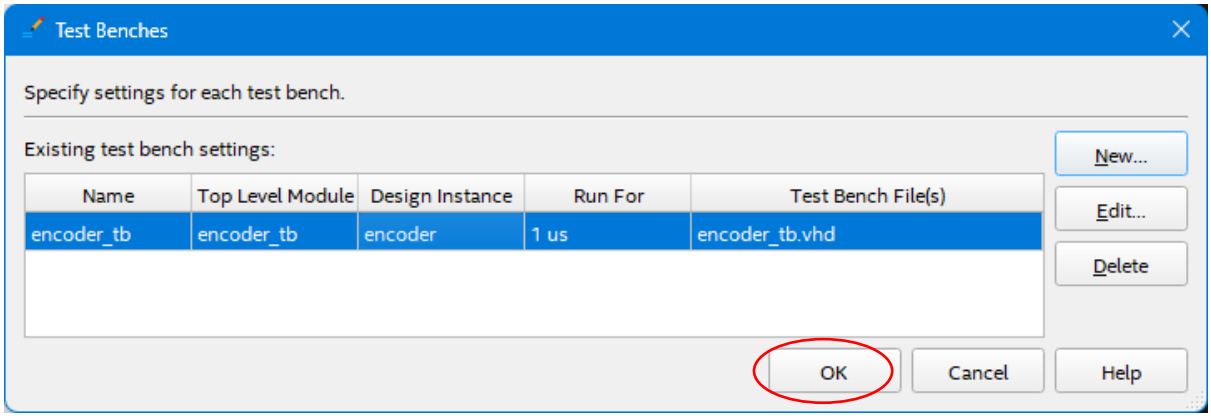


Select a new configuration



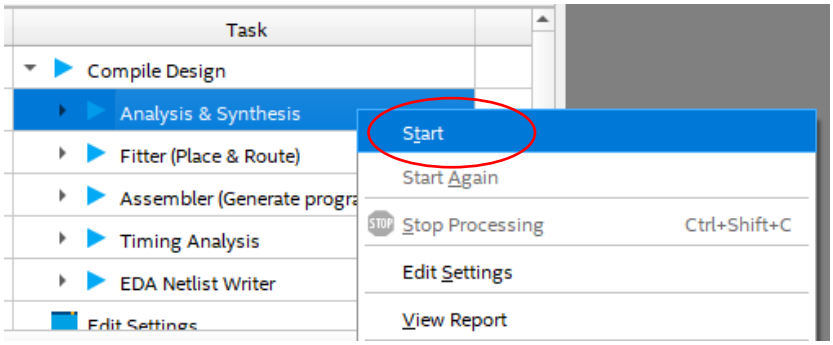
Find the testbench file on the disk (1),
Enter the name of the main unit defined in this file (2),
Select the use of testbench also for time simulation (3),
Set the simulation duration (4).



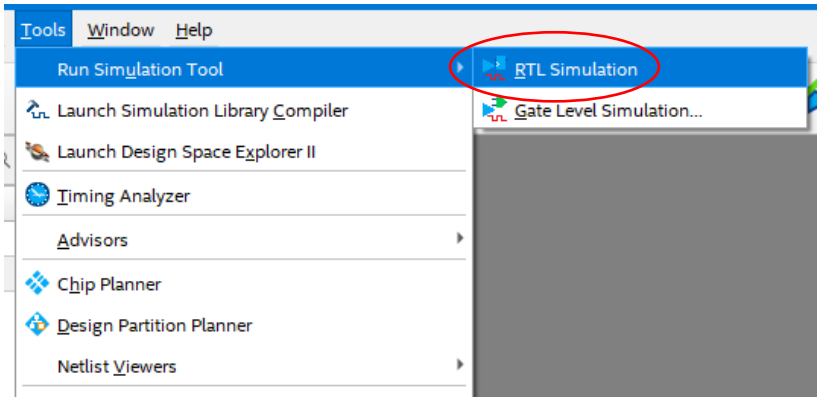


4. Starting the RTL simulation

Before performing RTL simulation, the project must be compiled.
From the Task window, from the Compile Design group, run the Analusis & Synthesis command

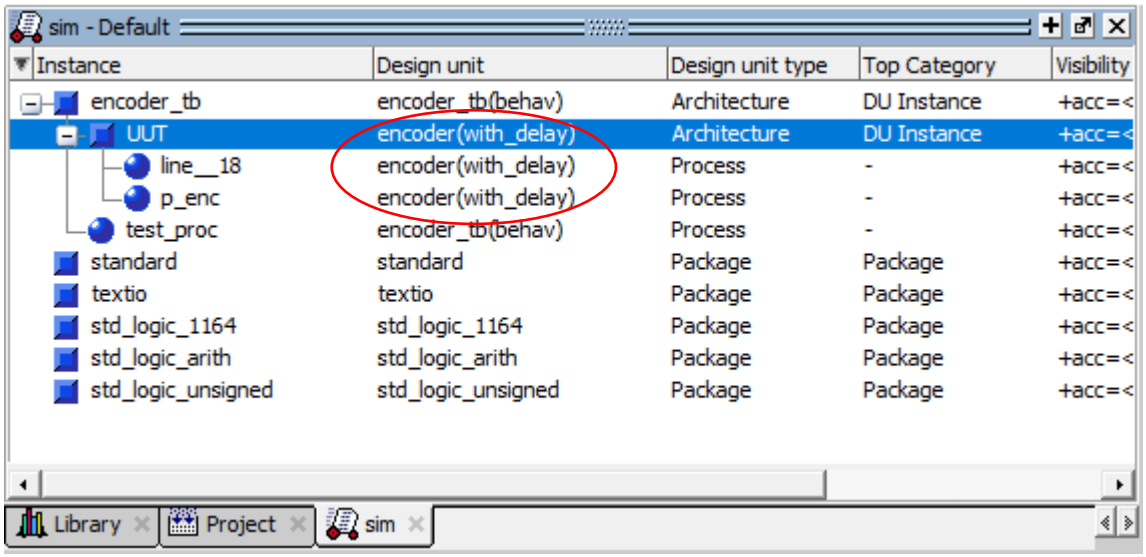


If the compilation was successful, run the RTL simulation from the Tools menu



As a result of this command, an external simulator will be opened and the configuration/simula-tion script defined in point 3 will be executed. The effects of the simulator operation can be observed in the "wave" time waveform window.

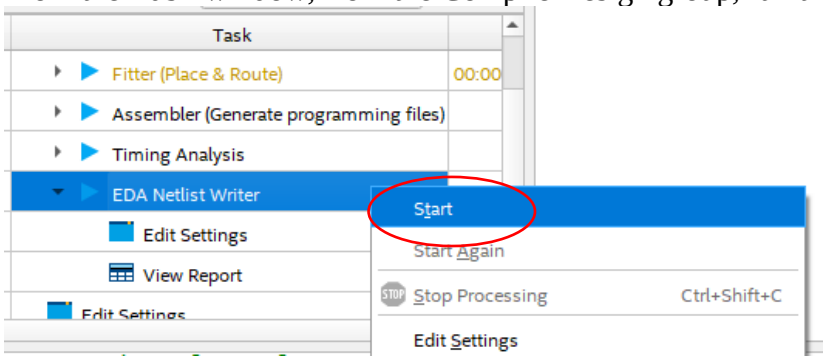
Verify the structure of the created project - the content of the "structure" (UUT) window should present the elements of the behavioral description from the encoder.vhd file



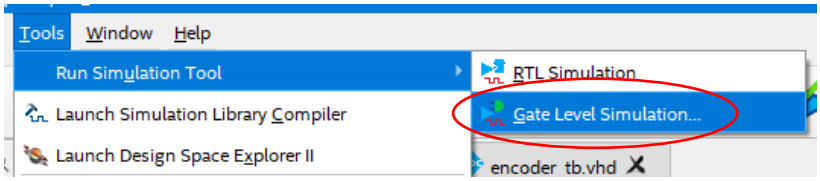
5. Starting the gate-level simulation

Before performing gate-level simulation, the project must pass the routing stage (Fitter – Place&Route). Then, start creating a model for simulation.

From the **Task** window, from the Compile Design group, run the **EDA Netlist Writer** command



If the netlist creation was successful, run the gate-level simulation from the **Tools** menu



As a result of this command, the external simulator will be opened and the configuration/simulation script defined in point 3 will be executed.

Verify the structure of the created project - the content of the "structure" window should present blocks of the automatically created structural model from the encoder.vho file