

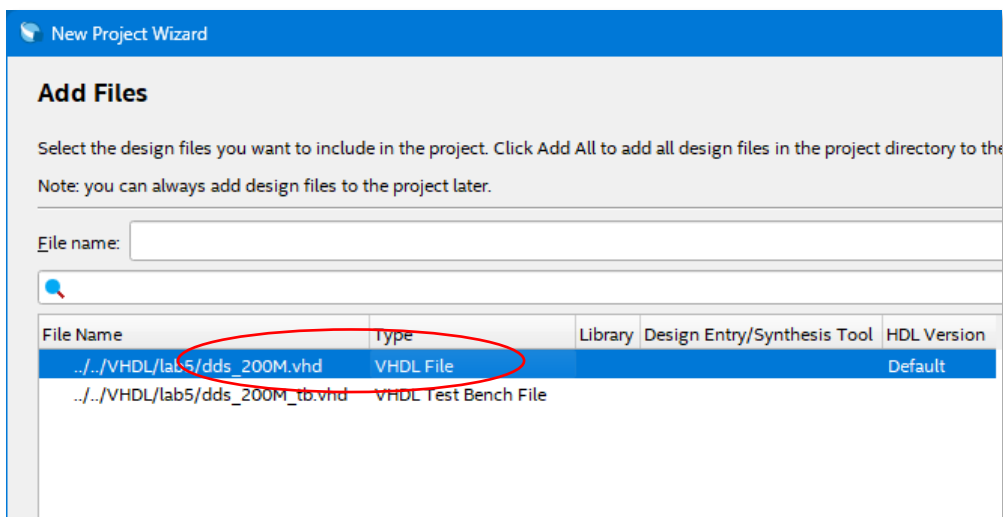
## Quartus Prime – IP catalog

### 1. Exercise goals

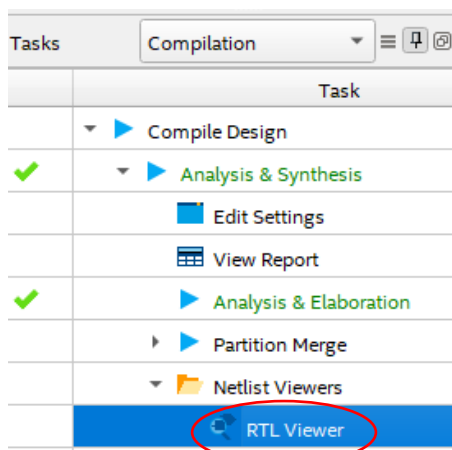
- a. The use of IP components in the construction of digital circuits
- b. Simulation using I/O files
- c. Implementation and testing on the FPGA platform

### 2. Simulation using IO files

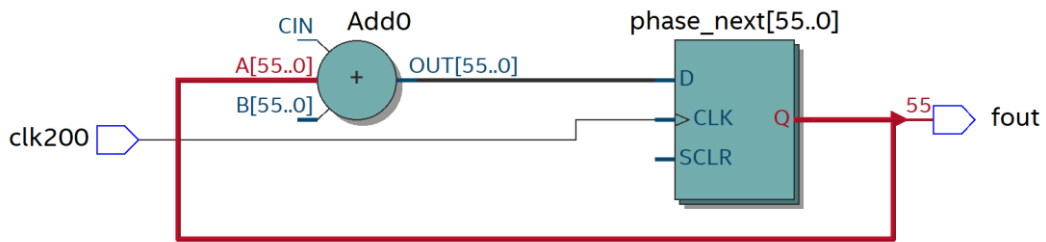
[!] Create a new Quartus Prime project and add files **.vhd** from the course server



[!] Perform **analysis** and **synthesis** of entity **dds\_200M**, get to know the structure of the system by viewing the diagram at the RTL level

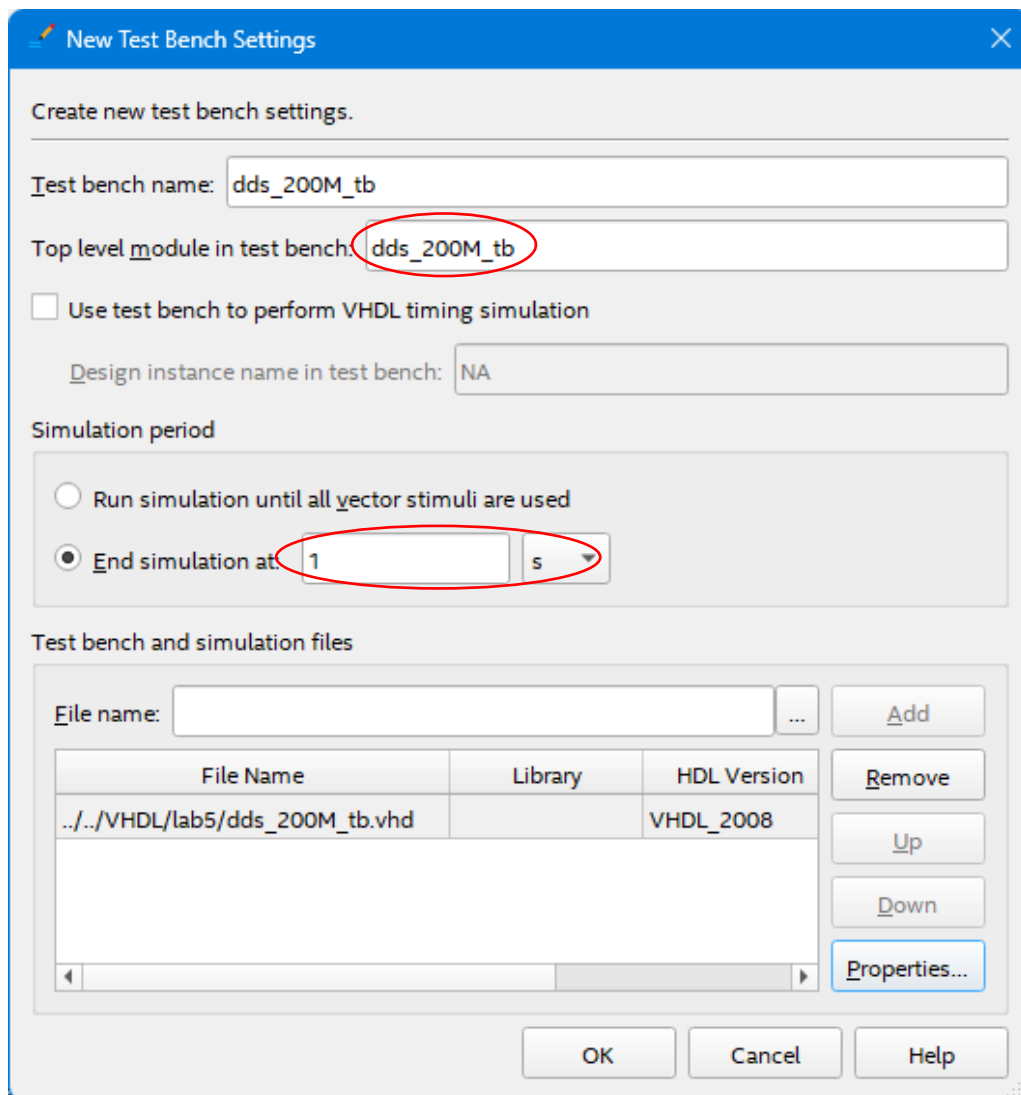


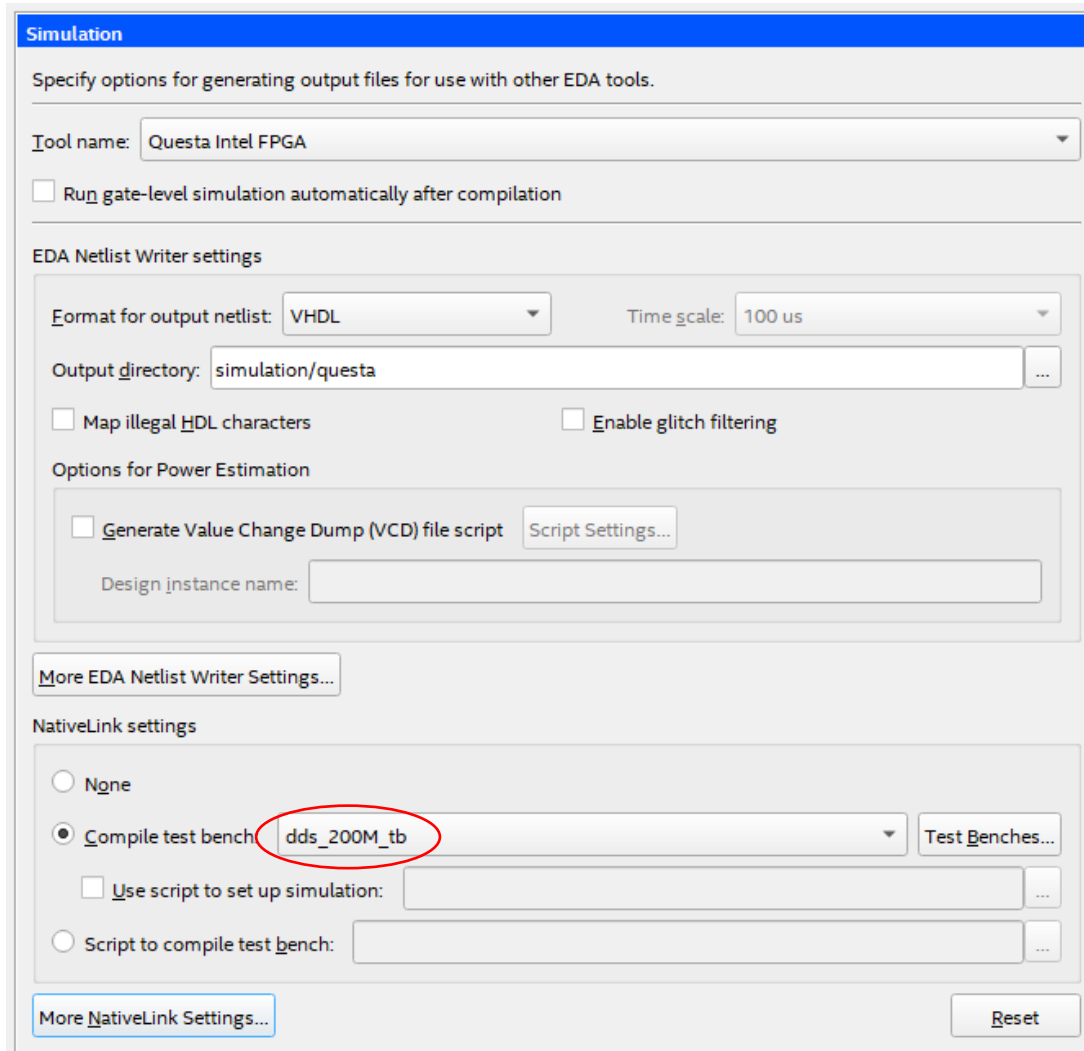
The internal structure of the system should include a phase accumulator of the programmable frequency generator as shown in the figure below



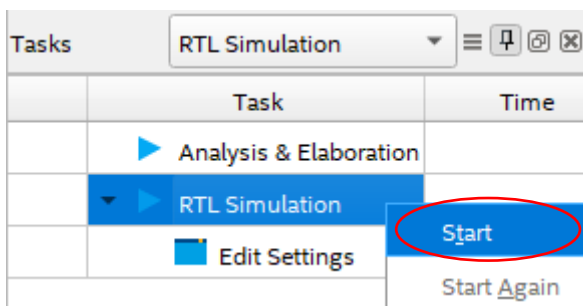
[!] Configure RTL simulation using testbench **dds\_200M\_tb**

Review the testbench code, check how to save the results to the output file.





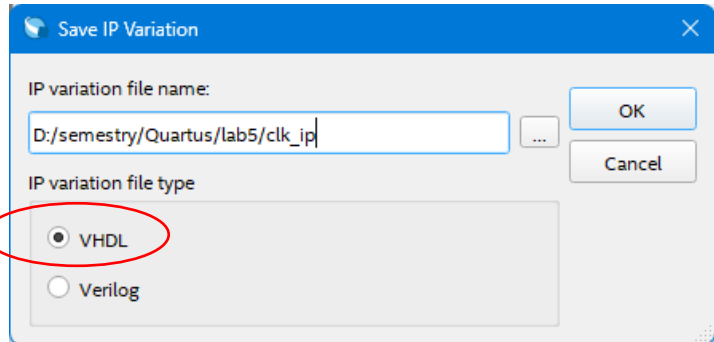
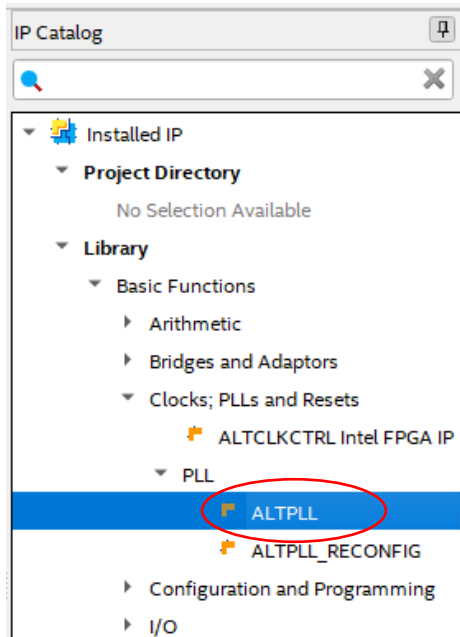
[!] Run RTL simulation for 1 second of device operating time



After running the simulation, [plot a histogram](#) based on the data in the output file (from the `.\simulation\questa` directory). Determine what component frequencies the tested DDS system generates.

### 3. Preparing the PLL clock generator

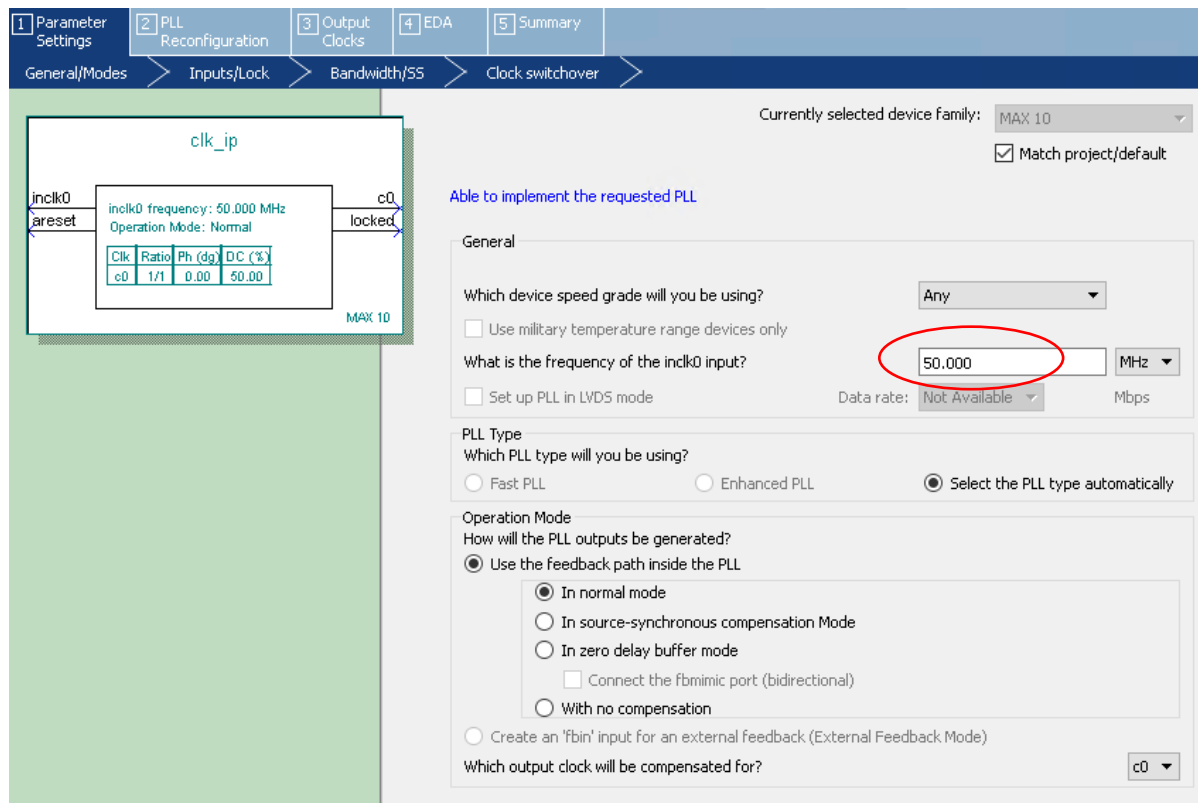
[!] Using the Quartus Prime IP component catalog prepare a 200MHz input clock generator



Make the settings on pages 1 and 6 of the Settings Manager. Leave the rest of the settings at default.

Page 1: 50MHz

Page 6: 200MHz



1 Parameter Settings | 2 PLL Reconfiguration | 3 Output Clocks | 4 EDA | 5 Summary

clk c0 > clk c1 > clk c2 > clk c3 > clk c4

clk\_ip

inclk0      areset      c0      locked

inclk0 frequency: 50.000 MHz  
Operation Mode: Normal

Clk	Ratio	Ph (dg)	DC (%)
c0	4/1	0.00	50.00

MAX 10

### c0 - Core/External Output Clock

Able to implement the requested PLL

Use this clock

Clock Tap Settings

- Enter output clock frequency:
 

200.00000000	MHz
--------------	-----
- Enter output clock parameters:
  - Clock multiplication factor: 1
  - Clock division factor: 1
- Clock phase shift: 0.00 deg
- Clock duty cycle (%): 50.00

Requested Settings	Actual Settings
200.00000000 MHz	200.000000
1	4
1	1
0.00 deg	0.00
50.00	50.00

Description	Value
Primary clock VCO frequency (MHz)	600.000
Modulus for M counter	12
Modulus for N counter	1

Note: The displayed internal settings of the PLL is recommended for use by advanced users only

Per Clock Feasibility Indicators

c0   c1   c2   c3   c4

Generated IP core interface (VHDL code)

```

43 ENTITY clk_ip IS
44     PORT
45     (
46         areset      : IN STD_LOGIC := '0';
47         inclk0      : IN STD_LOGIC := '0';
48         c0           : OUT STD_LOGIC ;
49         locked      : OUT STD_LOGIC
50     );
51 END clk_ip;

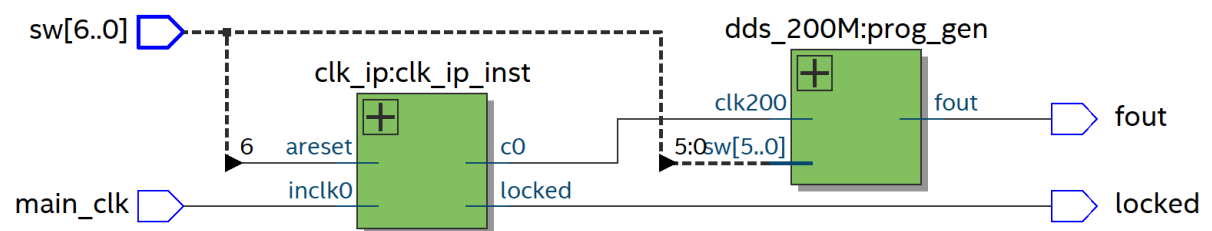
```

#### 4. Device integration

[!] Create a new main level design unit according to the given specification

```
11 entity top_dds_200M is
12     Port ( main_clk : in  STD_LOGIC; -- DE10-Lite 50MHz
13           sw : in  STD_LOGIC_VECTOR (6 downto 0); -- one hot
14           locked : out std_logic; -- ledr[0]
15           fout : out  STD_LOGIC); -- gpio[0]
16 end top_dds_200M;
```

[!] Place the generated IP core in the system, connect the 200MHz clock to the input of the DDS\_200M block.



#### 5. Pin assignment

[!] Assign the pins of the system according to the attached specification:

out locked	PIN_A8
in sw[4]	PIN_A12
in sw[6]	PIN_A13
in sw[5]	PIN_B12
in sw[0]	PIN_C10
in sw[1]	PIN_C11
in sw[3]	PIN_C12
in sw[2]	PIN_D12
in main_clk	PIN_P11
out fout	PIN_V10

Use Pin Planner or Assignment Editor for this purpose. All pins in the **3V3-LVTTL** standard.

Report

Report not available

Groups Report

Tasks

- Early Pin Planning
  - Early Pin Planning...
  - Run I/O Assignment Analysis
  - Export Pin Assignments...
- Pin Finder...
- Highlight Pins
  - I/O Banks
  - VREF Groups
  - Edges

Top View - Wire Bond

MAX 10 - 10M50DAF484C6GES

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current
fout	Output	PIN_V10	3	B3_NO	PIN_A7	3.3-V LVTTTL		8mA (d)
locked	Output	PIN_A8	7	B7_NO	PIN_R2	3.3-V LVTTTL		8mA (d)
main_clk	Input	PIN_P11	3	B3_NO	PIN_R11	3.3-V LVTTTL		8mA (d)
sw[6]	Input	PIN_A13	7	B7_NO	PIN_A13	3.3-V LVTTTL		8mA (d)
sw[5]	Input	PIN_B12	7	B7_NO	PIN_B12	3.3-V LVTTTL		8mA (d)
sw[4]	Input	PIN_A12	7	B7_NO	PIN_A12	3.3-V LVTTTL		8mA (d)
sw[3]	Input	PIN_C12	7	B7_NO	PIN_C12	3.3-V LVTTTL		8mA (d)
sw[2]	Input	PIN_D12	7	B7_NO	PIN_D12	3.3-V LVTTTL		8mA (d)
sw[1]	Input	PIN_C11	7	B7_NO	PIN_C11	3.3-V LVTTTL		8mA (d)
sw[0]	Input	PIN_C10	7	B7_NO	PIN_C10	3.3-V LVTTTL		8mA (d)

## 6. Prototype testing

[!] Perform assembly and program the **DE10-Lite** platform.

Connect the oscilloscope probe to the GPIO[0]. Test the operation of the system for different **SW** combinations.