

Quartus Prime – IP catalog

1. Exercise goals

- a. The use of IP components in the construction of digital circuits
- b. Simulation using I/O files
- c. Implementation and testing on the FPGA platform

2. Simulation using IO files

[!] Create a new Quartus Prime project and add files .vhd from the course server

🕞 New Project Wizard				
Add Files				
Select the design files you want to includ	le in the project. Click Add	All to ad	ld all design files in the project	t directory to the
Note: you can always add design files to	the project later.			
<u>F</u> ile name:				
File Name	Туре	Library	Design Entry/Synthesis Tool	HDL Version
//VHDL/lak5/dds_200M.vhd	VHDL File			Default
//VHDL/lab5/dds_200M_tb.vhd	VHDL Test Bench File			

[!] Perform analysis and synthesis of entity dds_200M, get to know the structure of the system by viewing the diagram at the RTL level



The internal structure of the system should include a phase accumulator of the programmable frequency generator as shown in the figure below



[!] Configure RTL simulation using testbench dds_200M_tb

Review the testbench code, check how to save the results to the output file.

New Test Bench Settings			×	
Create new test bench settings.				
Test bench name: dds_200M_tb				
Top level module in test bench. dds_20	0M_tb			
Use test bench to perform VHDL timir	ng simulation			
Design instance name in test bench:	NA			
Simulation period				
Run simulation until all <u>v</u> ector stim <u>E</u> nd simulation at	uli are used			
<u>F</u> ile name:			Add	
File Name	Library	HDL Version	<u>R</u> emove	
//VHDL/lab5/dds_200M_tb.vhd		VHDL_2008	Цр	
			Down	
•		Þ	Properties	
	ОК	Cancel	Help	

Simulation				
Specify options for generating output files for use with other EDA tools.				
Tool name: Questa Intel FPGA	•			
Run gate-level simulation automatically after compilation				
EDA Netlist Writer settings				
Eormat for output netlist: VHDL Time scale: 100 us	s v			
Output directory: simulation/questa				
Map illegal <u>H</u> DL characters <u>E</u> nable glitch filtering				
Options for Power Estimation				
Generate Value Change Dump (VCD) file script Script Settings				
Design instance name:				
More EDA Netlist Writer Settings				
<u>C</u> ompile test bench dds_200M_tb	▼ Test <u>B</u> enches			
Use script to set up simulation:				
O Script to compile test <u>b</u> ench:				
More <u>N</u> ativeLink Settings	Reset			

[!] Run RTL simulation for 1 second of device operating time

Tasks	RTL Simulation	- ₽ Ø ×
	Task	Time
	Analysis & Elaboration	
	RTL Simulation	
	Edit Settings	S <u>t</u> art
		Start <u>A</u> gain

After running the simulation, plot a histogram based on the data in the output file (from the .\simulation\questa directory). Determine what component frequencies the tested DDS system generates.

3. Preparing the PLL clock generator

[!] Using the Quartus Prime IP component catalog prepare a 200MHz input clock generator



Make the settings on pages 1 and 6 of the Settings Manager. Leave the rest of the settings at default.

Page 1: 50MHz

Page 6: 200MHz

1 Parameter Settings	2 PLL Reconfiguration	3 Output 4 f Clocks		5 Summary				
General/Modes	Inputs/Lock	Bandwidth/SS	>	Clock switchover	>			
					Currently	selected device family:	MAX 10	Ψ.
	clk_ip						🗹 Match proje	ect/default
inclk0 incl	(0 frequency: 50.000 MHz	c0	Able	to implement the r	equested PLL			
	ration Mode: Normal Ratio Ph (dg) DC (%)	IDERCU.	Ger	neral				
	1/1 0.00 50.00		WH	ich device speed (grade will you be using?	Any	•	·
L		MAX ID		Use military temp	erature range devices only			
			WH	iat is the frequenc	y of the inclk0 input?	50.000		MHz 🔻
				Set up PLL in LVD:	5 mode	Data rate: Not Avail	able 🔻	Mbps
			PLL	. Type iich PLL type will y	ou be using?			
				Fast PLL	O Enhanced PLL	Selection	t the PLL type at	utomatically
			Ор	eration Mode	uts be generated?			
			۲	Use the feedback	path inside the PLL			
				In norr	nal mode			
				O In sou	rce-synchronous compensation M	lode		
				O In zero) delay butter mode	n all		
				O With n	o compensation	(lai)		
				Create an 'fbin' ir	put for an external feedback (E>	(ternal Feedback Mode)		
			WH	ich output clock w	ill be compensated for?			c0 🔻

1 Parameter 2 PLL 3 Output Settings Reconfiguration Clocks	4 EDA	5 Summary				
<u>clkc0</u> clkc1 > clkc2 > clkc3	> c1k c4 >					
Clk_ip inclk0 requency: 50.000 MHz Operation Mode: Normal Clk Ratio Ph (dg) DC (%) c0 4/1 0.00 50.00 MAX	CO - 1 Able to Occk ed 0 Er 0 Clock Clock	Core/External Ou implement the requested if this clock Tap Settings ner output clock frequency ner output clock parameter Clock multiplication factor Clock division factor phase shift duty cycle (%)	rs:	Requested Settings 200.00000000 1 ↓ 1 ↓ 0.00 ↓ 50.00	Actual Settings 200.000000 4 1 0.00 50.00	
	Note: PLL is users	The displayed internal sett recommended for use by a only	ings of the f idvanced f	Description Primary clock VCO frequency (MHz) Modulus for M counter Modulus for N counter Per Clock Feasibility In CD C1 C2 C	Value 600.000 12 1 v dicators 3 c4	

Generated IP core interface (VHDL code)

43	ENTITY	clk_ip I	s				
44	PO	RT					
45	(
46		areset		1.1	IN STD_LOGIC	:=	'0';
47		inclk0		1	IN STD_LOGIC	:=	'0';
48		c0	1	OUT	STD_LOGIC ;		
49		locked		1	OUT STD_LOGIC		
50	-);						
51	LEND cl	k_ip;					

4. Device integration

[!] Create a new main level design unit according to the given specification

```
11 Pentity top_dds_200M is
12 Port ( main_clk : in STD_LOGIC; -- DE10-Lite 50MHz
13 sw : in STD_LOGIC_VECTOR (6 downto 0); -- one hot
14 locked : out std_logic; -- ledr[0]
15 fout : out STD_LOGIC); -- gpio[0]
16 end top_dds_200M;
```

[!] Place the generated IP core in the system, connect the 200MHz clock to the input of the DDS_200M block.



5. Pin assignment

[!] Assign the pins of the system according to the attached specification:

out locked	PIN_A8
in sw[4]	PIN_A12
in sw[6]	PIN_A13
in sw[5]	PIN_B12
in sw[0]	PIN_C10
in sw[1]	PIN_C11
in sw[3]	PIN_C12
in sw[2]	PIN_D12
in_ main_clk	PIN_P11
out fout	PIN_V10

Use Pin Planner or Assignment Editor for this purpose. All pins in the **3V3-LVTTL** standard.



6. Prototype testing

[!] Perform assembly and program the **DE10-Lite** platform.

Connect the oscilloscope probe to the GPIO[0]. Test the operation of the system for different **SW** combinations.