Custom Computing & Embedded Systems

Quartus Prime – HW debug

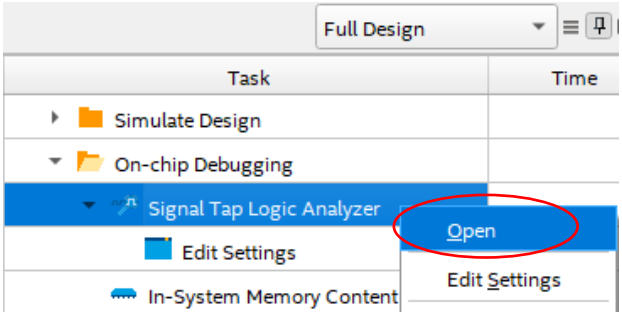
1. Exercise goals

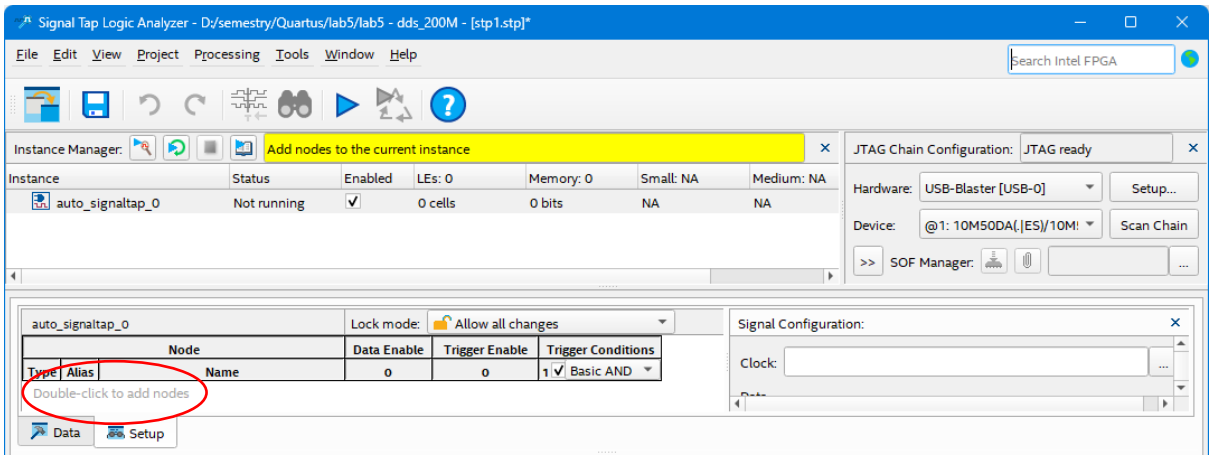
a. The use of IP components in the construction of digital circuits
b. Testing the prototype on the FPGA platform
c. Use of integrated analyzers

2. Preparing the debugging interface

[!] Open the Quartus project Prime prepared in the previous exercise (lab5)

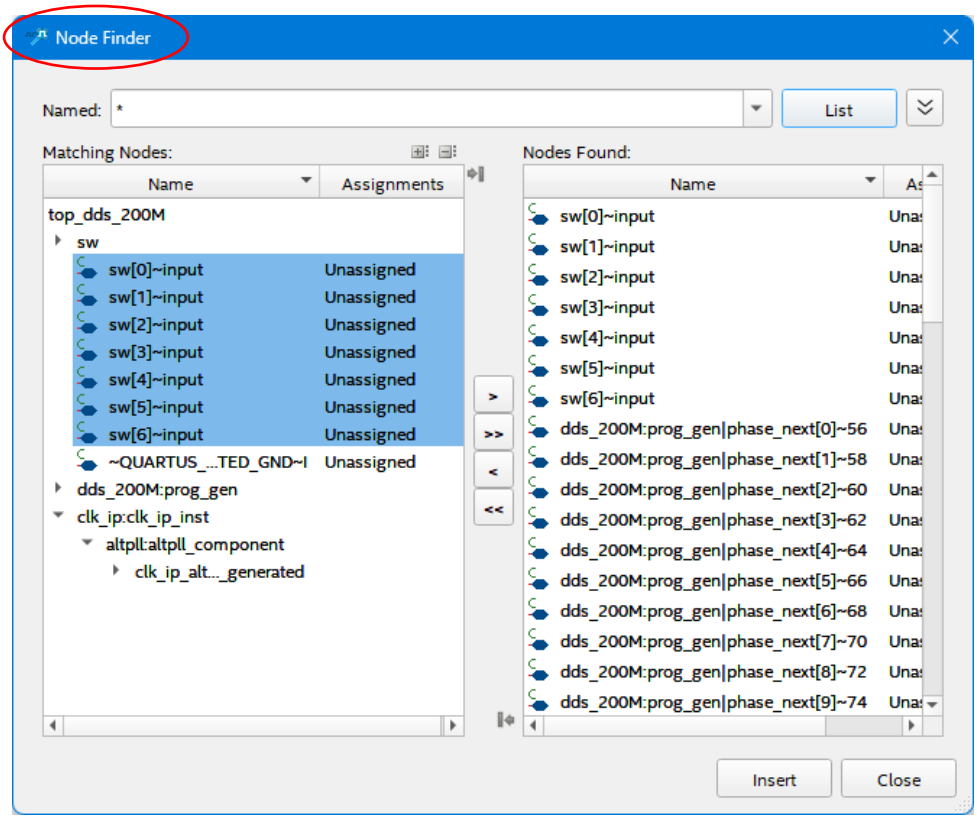
Open **Signal Tap Logic Analyzer** from the **Tasks** window



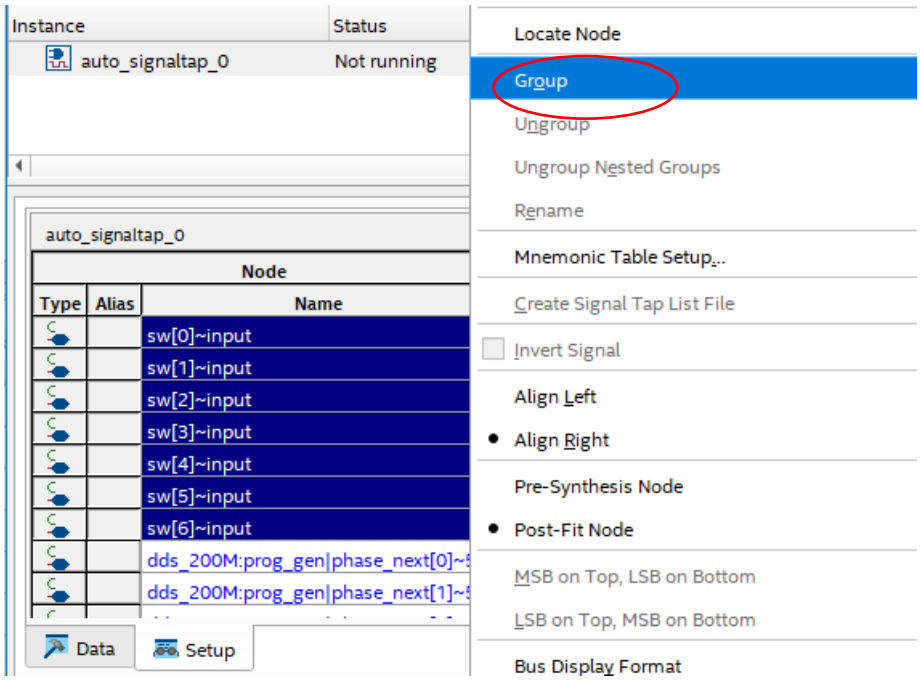


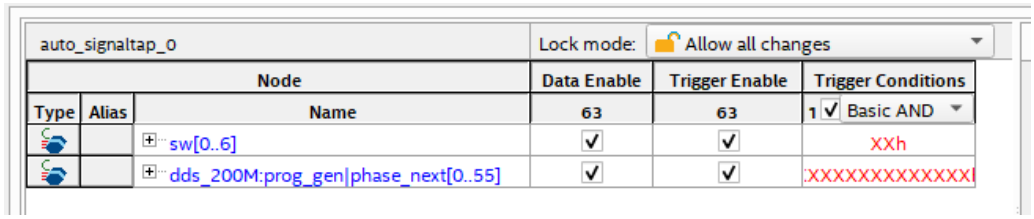
Add signals (double-click in Setup) to the settings window using **Node Finder**

Add all SW and phase_next signals to the Node list

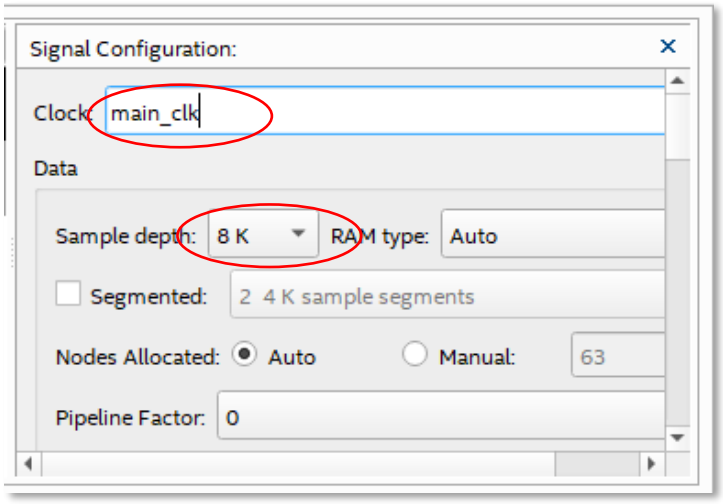


Perform signal grouping using the context menu (RMB)



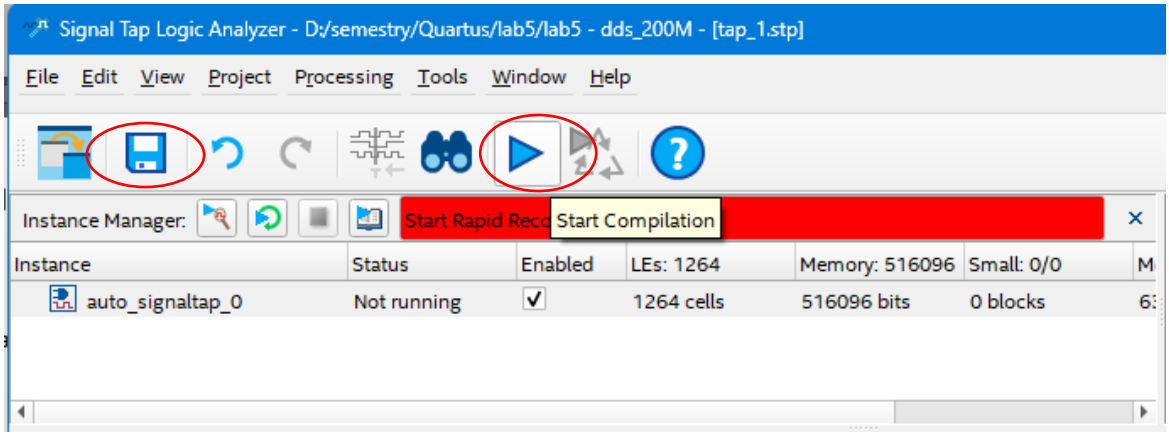


Set the sample memory depth to 8k and the sample clock to main_clk



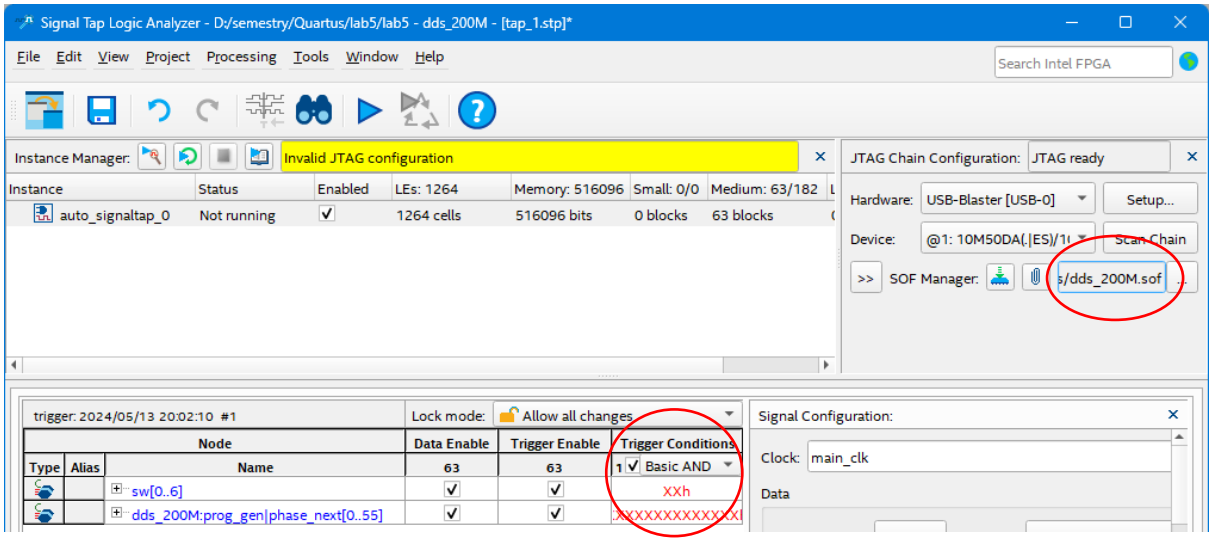
[!] Save changes to **tap_1.stp**

[!] Run the system recompilation and generate a new bitstream for programming the FPGA

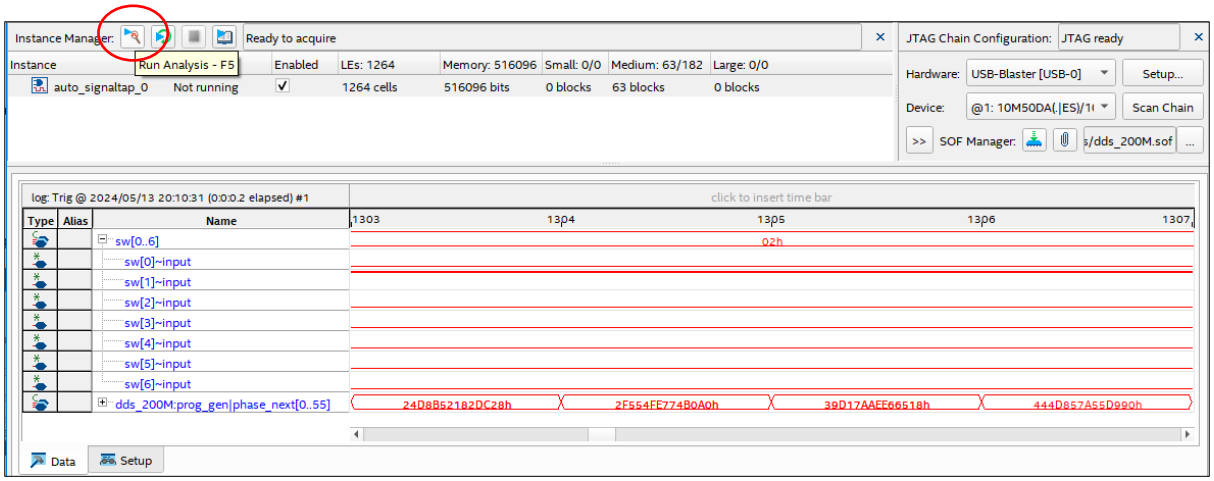


3. Prototype testing

[!] Program the system using the **Signal Tap Logic Analyzer**
Set the **dds_200M.sof** programming file in the **JTAG Chain Configuration** interface



[!] Start signal measurement without setting trigger conditions
(**Trigger Condition** in the **Setup window** = XX)



Task A

- Test **pattern triggering** and **signal level triggering**
- Modify the ILA settings to measure the output signal (fout).
- Measure and calculate the fout frequency for **SW** =”000010”