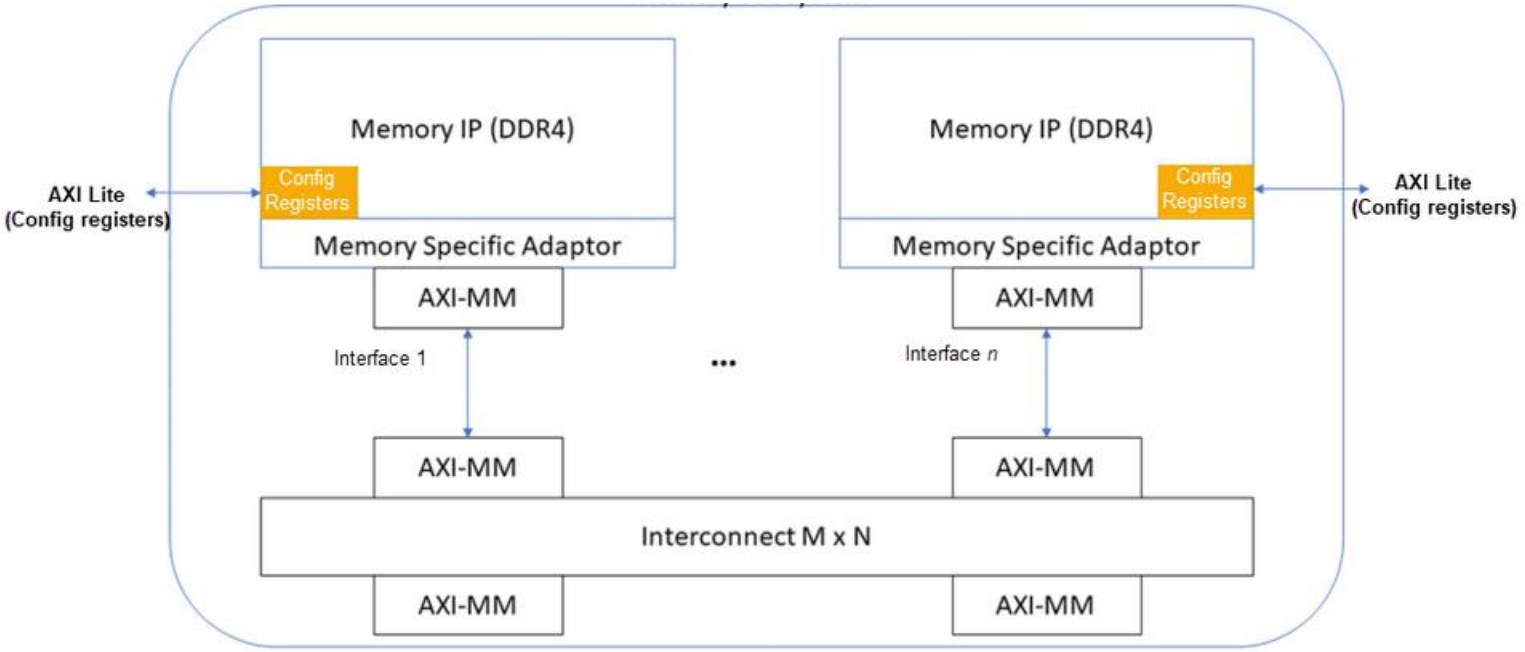
Embedded Systems
Hardware Design

Memory subsystems

Memory subsystem

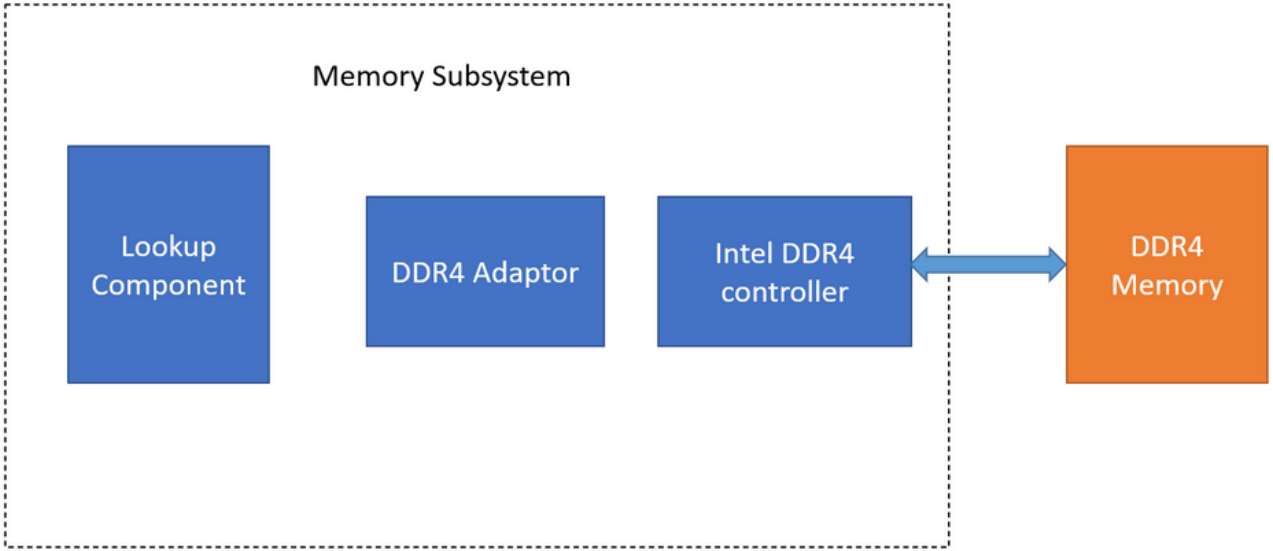
The memory subsystem IP is a high-level solution on top of the External Memory Interfaces.



Source https://www.intel.com/content/www/us/en/docs/programmable/789389/24-1-2-0-0/introduction-to-memory-subsystem-ip.html

Memory Subsystem IP Used as Memory Adaptor with Lookup and One EMIF

The memory subsystem IP can be configured for use in various applications such as full crossbar for machine learning, multi-hierarchy memory bridge, or as a memory-specific adaptor with lookup core logic. All the available modes offer common scalability and compose-ability.



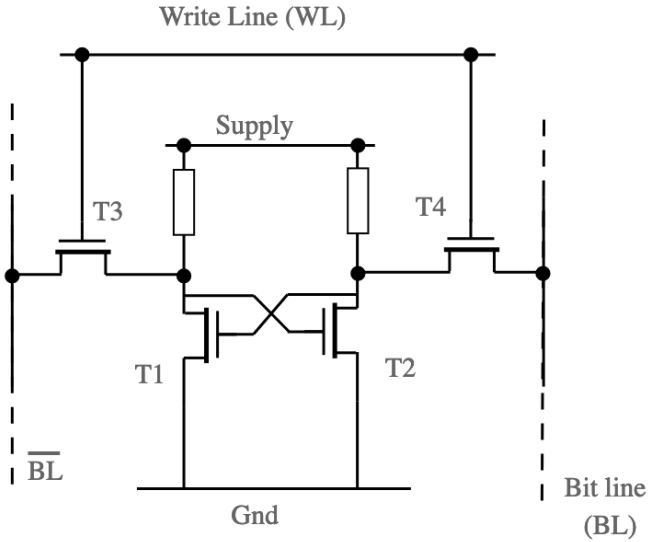
Source https://www.intel.com/content/www/us/en/docs/programmable/789389/24-1-2-0-0/introduction-to-memory-subsystem-ip.html

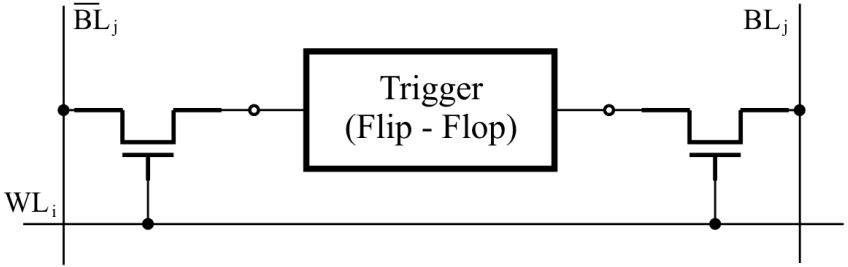
Types

- ROM
  - PROM
  - EPROM
  - EEPROM
- RAM
  - SRAM
  - DRAM
    - Synchronous
    - DDR – Double data rate
  - NVRAM (non-volatile RAM)

Static RAM

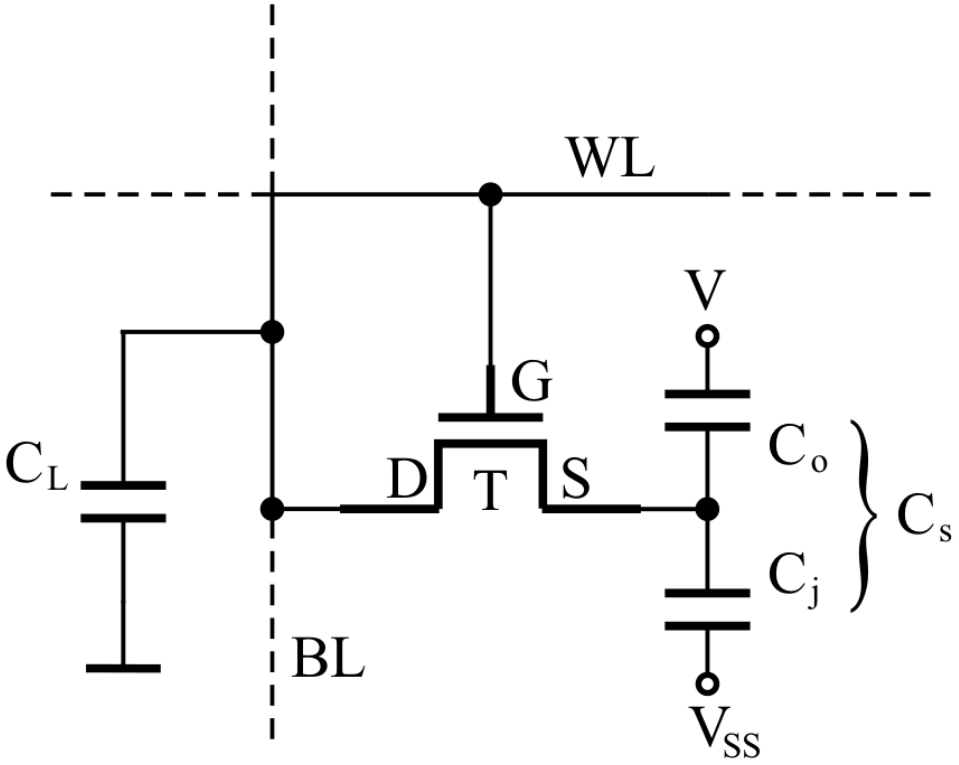
- Uses SR-Latches
- Expensive
- Doesn't need refreshing



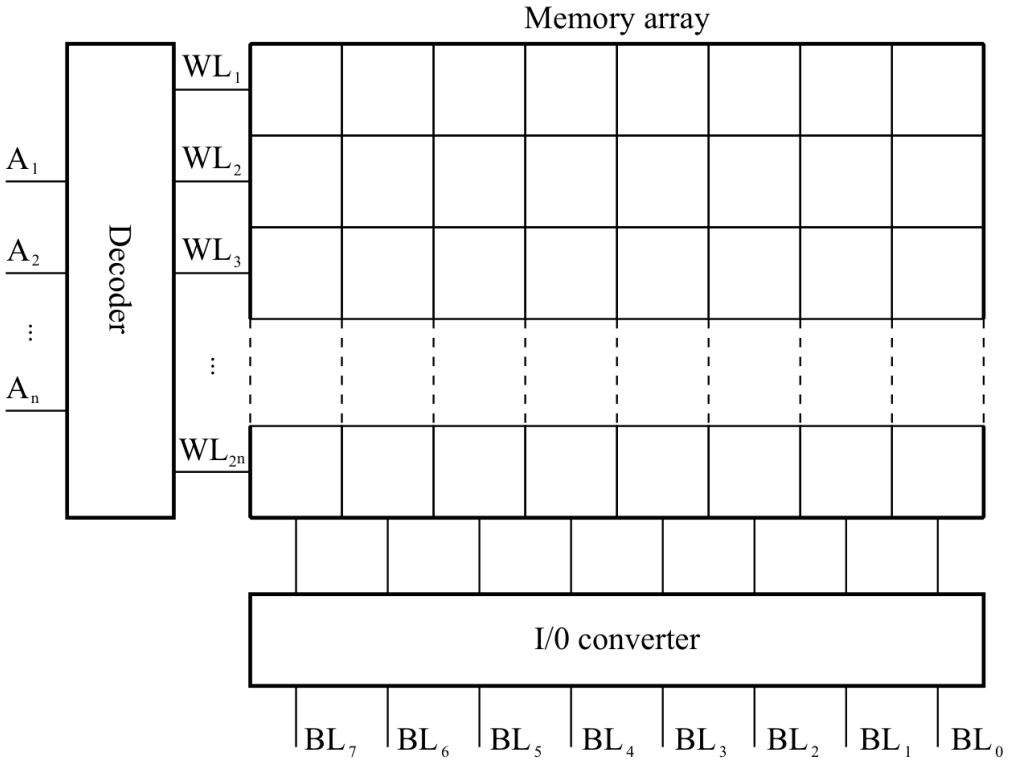


Dynamic RAM

- Uses small capacitors (with transistors)
- Requires constant refreshing
- Cheap



Digital memory architecture



Max supported memory & the ‘4GB limit’

- Address lines ~ Bits
- 16 bit => 216 = 65,536 bytes (64 KiB)
- 32 bit => 232 = 4,294,967,296 bytes (4 GiB)
- 64 bit => 264 = 18,446,744,073,709,551,616 bytes (16 EiB)
- KiB ≠ KB, GiB ≠ GB, EiB ≠ EB
  - KB, MB, GB, PB, EB – 1000 as a base
  - KiB, MiB, GiB, PiB, EiB – 1024 as a base
  - 1 MB = 0.953 MiB
  - 1.073 TB = 1 TiB

PAE

- Physical address extension
- Allows 32-bit OS to address more than 4GiB of memory
  - From 2^{32} to 2^{36} bytes
- Requires OS, CPU and motherboard chipset support.
- e.g. 32bit OS - Windows Server 2008 Enterprise, Datacenter can address up to 64 GB of memory

RAM

- RAM – Random Access Memory
- DRAM – Dynamic RAM
- SRAM – Static RAM
- SDRAM - Synchronous DRAM
- DDR – Double Data Rate (data is transferred on both rising and falling edges of the system's memory clock)

(S)DRAM

- SDR SDRAM (Single Data Rate)
- DDR SDRAM (Double Data Rate)
- DDR2 SDRAM
- DDR3 SDRAM
- DDR4 SDRAM
- DDR5 SDRAM

Formfactors

- DIMM - Dual In-Line Memory Module
- SODIMM – Small Outline DIMM
- CAMM/LPCAMM - Compression Attached Memory Module
- Soldered

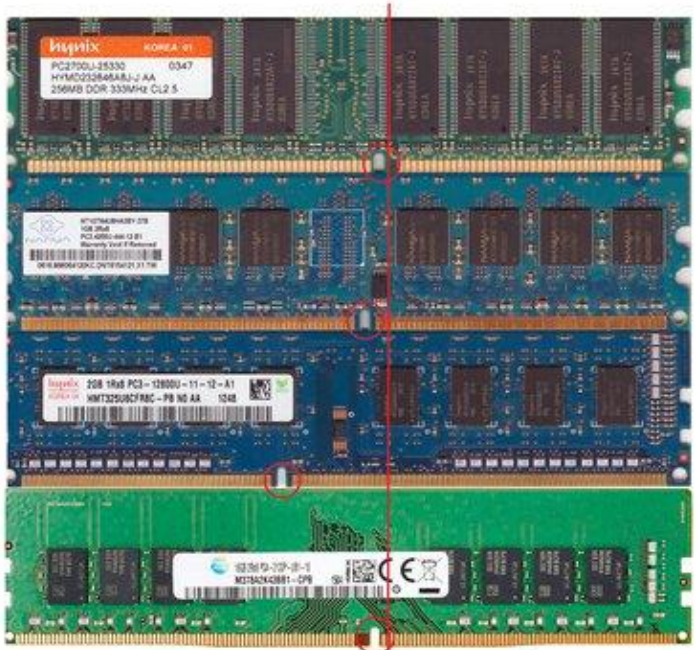
Physical Differences
DDR 1, 2, 3, 4 DIMMS

184 PINS — DDR 1

240 PINS — DDR 2

240 PINS — DDR 3

288 PINS — DDR 4

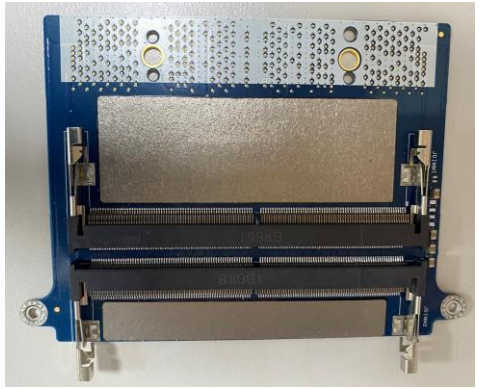


SODIMM

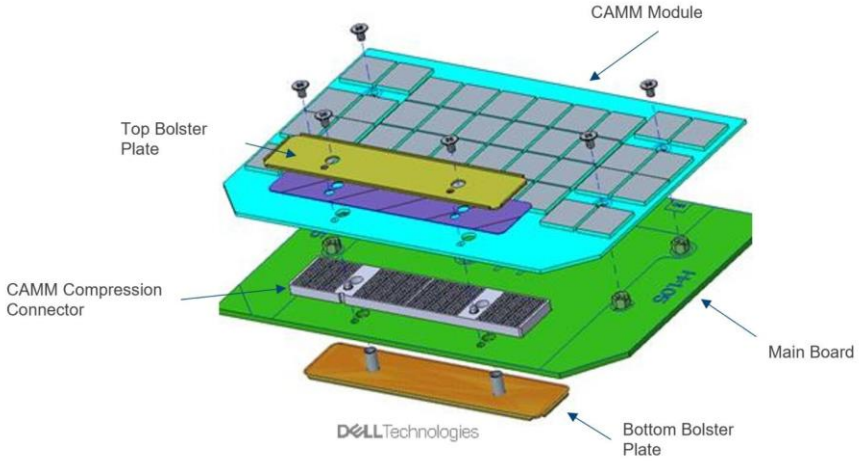
Every standard (SDRAM, DDR{1..5}) has its own SODIMM version – notch in different spots

SODIMM can be used in DIMM slot using an adapter – same signals, different form-factor

CAMM

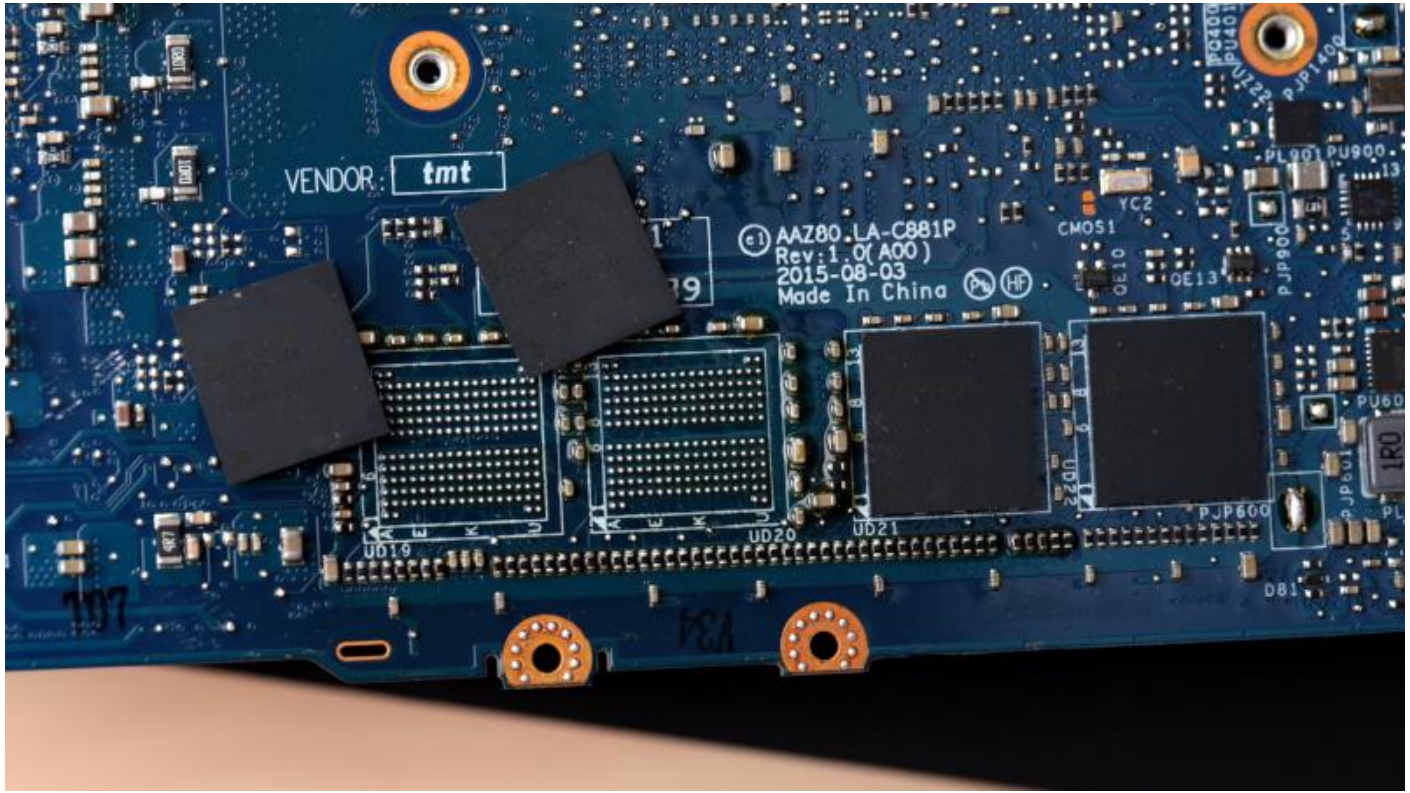


- Thinner than SODIMM (~57% thinner)
- Shorter traces (can be faster)
- Replacable/upgradable (vs soldered RAM)



Source: https://www.extremetech.com/computing/334676-dell-offers-additional-insight-on-its-new-camm-memory-modules

Soldered



Source: https://hackaday.com/2021/11/24/you-cant-upgrade-soldered-on-laptop-ram-think-again/

Voltage

- DDR (2.6V, 2.5V)
- DDR2 (1.8V)
- DDR3 (1.5V), DDR3L (1.35V)
- DDR4 (1.2V), ~~DDR4L (1.05V)~~
- DDR5 (1.1V)

DDR3L

- Lower required voltage – less power consumption
- Can work at both 1.35V and 1.5V (compatible with systems using DDR3 not ‘L’)
- Some systems doesn’t work with DDR3 and require DDR3L

LPDDR

- Low power DDR
- Aimed at mobile devices
- DDR3L vs LPDDR3
- LPDDR4(x)
- LPDDR5(x)
- LPDDR6 ~2024/2025

Properties of the different LPDDR generations

LPDDR	1	1E	2	2E	3	3E	4	4X	5	5X
Maximum density (bit)					32		64	64	32	32
Memory array clock (MHz)	200	266	200	266	200	266	200	266	400	533
Prefetch size	2*n*		4*n*		8*n*		16*n*			
Memory densities			64 Mbit – 8 Gbit		1–32 Gbit		4–32 Gbit		4–32 Gbit	
I/O bus clock frequency (MHz)	200	266	400	533	800	1067	1600	2133	3200	4267
Data transfer rate, DDR (MT/s)[a]	400	533	800	1067	1600	2133	3200	4267	6400	8533
Supply voltages (volts)	1.8		1.2, 1.8		1.2, 1.8		1.1, 1.8	0.6, 1.1, 1.8	0.5, 1.05, 1.8	0.5, 1.05, 1.8
Command/ address bus	19 bits, SDR		10 bits, DDR				6 bits, SDR		7 bits, DDR	
Year	2006		2009		2012		2014	2017	2019	2021

LPDDR in Samsung phones

- S23 (2022) LPDDR5X
- S21 (2020) LPDDR5
- S10 (2019) LPDDR4X
- S7 (2016) LPDDR4
- S5 (2014) LPDDR3
- S2 (2011) LPDDR2

Types

- UDIMM – unbuffered/unregistered DIMM
  - Most consumer memory
  - Rarely with ECC
- RDIMM – Registered DIMM
  - Additional register chip (buffer) is added between DRAM chips and MC.
  - Allows for more DRAM chips on one DIMM
    (reduces electrical load on the control lines)
  - Usually has ECC capabilities
- LRDIMM – Load Reduced DIMM
  - Similar to RDIMM, but also data lines are buffered

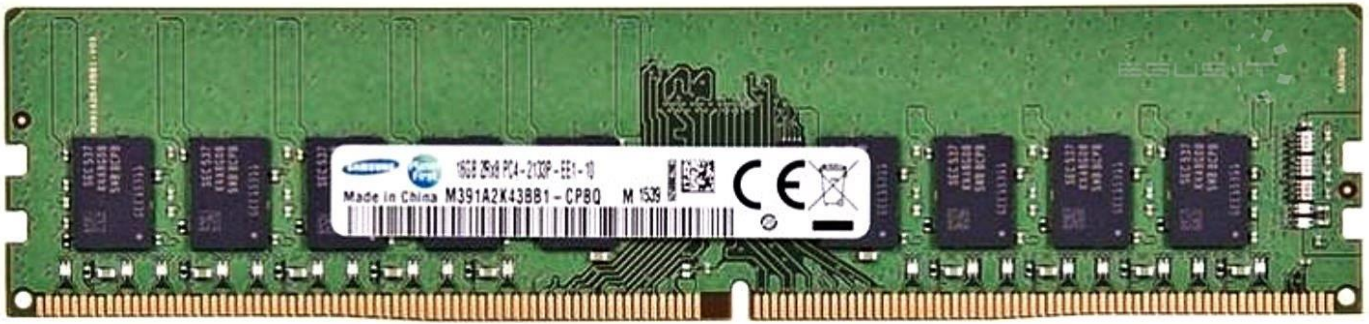
ECC memory

- ECC - Error correction codes
- Used to detect and fix memory errors
- Protects against ‘bit-flips’
  - 1-bit errors are detected and are transparently corrected
  - 2-bit errors are detected and cannot be corrected

Systems' memory requirements

- Some platforms require the use of RDIMM
  - Since DDR5: RDIMM is keyed differently to UDIMM
- UDIMM platform cannot use RDIMM
- Non-ECC UDIMM plaforms can still use ECC UDIMMs
- To use ECC of UDIMM - CPU and Chipset need to support ECC features.

UDIMM – ECC vs non-ECC



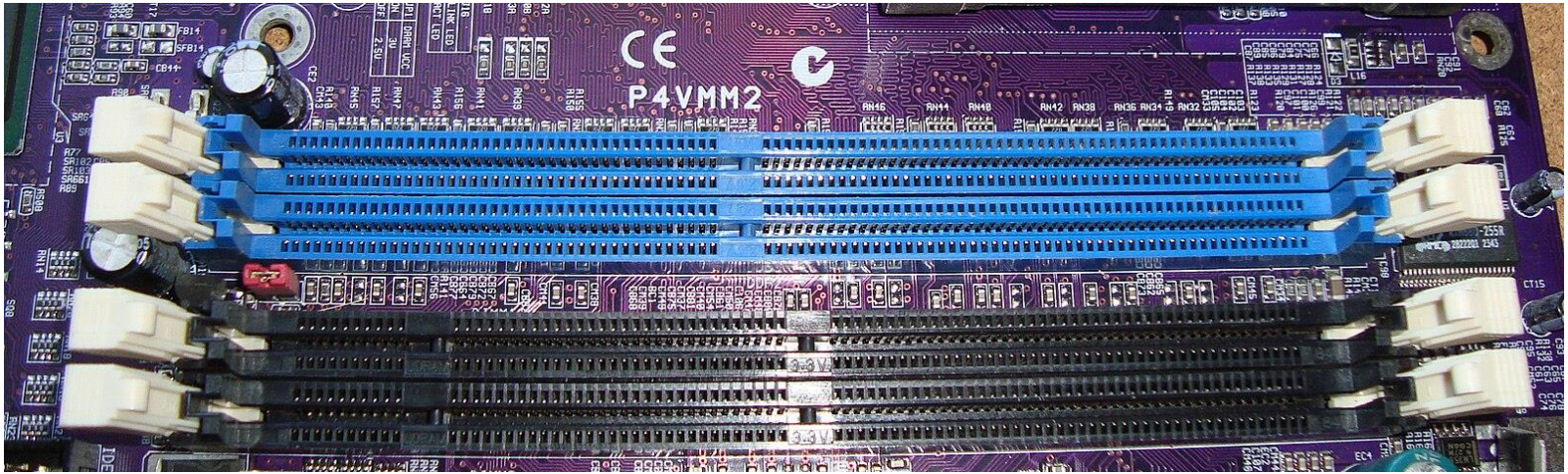
RDIMM

Aditional register chip (buffer) in the middle of a module

Supported Memory Type for Intel Core Desktop Processors

- DDR3: 1st – 7th gen
- DDR4: 6th – 14th gen
- DDR5: 12th – 14th gen
- Most CPUs support two memory standards
  - Only one can be used at one time
  - Different motherboards can use different memory type for the same CPU
- https://www.intel.com/content/www/us/en/support/articles/000094585/processors.html

Motherboards with two memory types

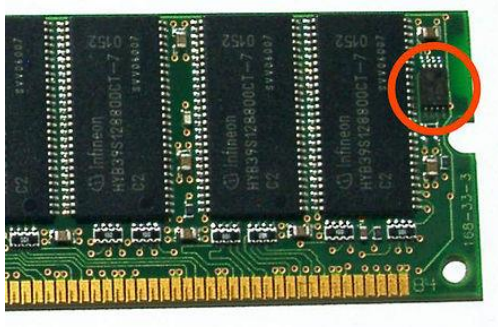


SDRAM and DDR(1) slots on P4VMM2
Only one type can be used at once (or it doesn't POST)

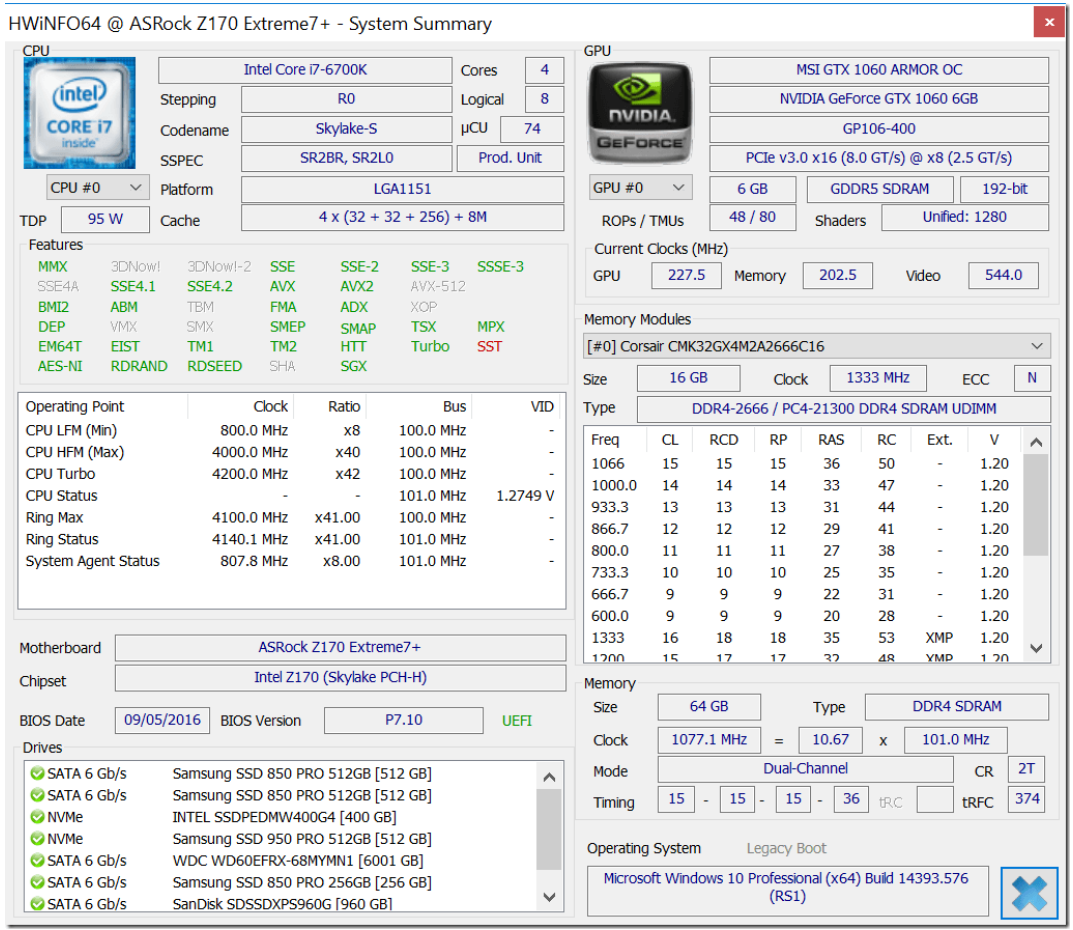
GDDR SDRAM

- GDDR Graphics Double Data Rate SDRAM
  - DDR SGRAM
  - GDDR2
  - GDDR3
  - GDDR4
  - GDDR5
  - GDDR6
  - GDDR7

Detection



- SPD – Serial presence detection
- Simply flash memory (EEPROM)
- Uses SMBUS (~I^2C, also for temp. sensors on DIMMs)
- Contains: model name, specifications, supported timings, (optionally) XMP timings (Extreme Memory Profile)
- JEDEC Standard 21-C section 4.1.2.4 "SPDs for DDR SDRAM"


HWiNFO64 @ ASRock Z170 Extreme7+ - System Summary
CPU
Intel Core i7-6700K
Cores 4
Stepping R0
Logical 8
Codename Skylake-S
µCU 74
SSPEC SR2BR, SR2L0
Prod. Unit
CPU #0
Platform LGA1151
TDP 95 W
Cache 4 x (32 + 32 + 256) + 8M
Features
MMX 3DNow! 3DNow!-2 SSE SSE-2 SSE-3 SSSE-3
SSE4A SSE4.1 SSE4.2 AVX AVX2 AVX-512
BMI2 ABM TBM FMA ADX XOP
DEP VMX SMX SMEP SMAP TSX MPX
EM64T EIST TM1 TM2 HTT Turbo SST
AES-NI RDRAND RDSEED SHA SGX
Operating Point Clock Ratio Bus VID
CPU LFM (Min) 800.0 MHz x8 100.0 MHz -
CPU HFM (Max) 4000.0 MHz x40 100.0 MHz -
CPU Turbo 4200.0 MHz x42 100.0 MHz -
CPU Status - - 101.0 MHz 1.2749 V
Ring Max 4100.0 MHz x41.00 100.0 MHz -
Ring Status 4140.1 MHz x41.00 101.0 MHz -
System Agent Status 807.8 MHz x8.00 101.0 MHz -
Motherboard ASRock Z170 Extreme7+
Chipset Intel Z170 (Skylake PCH-H)
BIOS Date 09/05/2016
BIOS Version P7.10
UEFI
Drives
SATA 6 Gb/s Samsung SSD 850 PRO 512GB [512 GB]
SATA 6 Gb/s Samsung SSD 850 PRO 512GB [512 GB]
NVMe INTEL SSDPEDMW400G4 [400 GB]
NVMe Samsung SSD 950 PRO 512GB [512 GB]
SATA 6 Gb/s WDC WD60EFRX-68MYMN1 [6001 GB]
SATA 6 Gb/s Samsung SSD 850 PRO 256GB [256 GB]
SATA 6 Gb/s SanDisk SDSSDXPS960G [960 GB]
GPU
MSI GTX 1060 ARMOR OC
NVIDIA GeForce GTX 1060 6GB
GP106-400
PCIe v3.0 x16 (8.0 GT/s) @ x8 (2.5 GT/s)
GPU #0
6 GB
GDDR5 SDRAM
192-bit
ROPs / TMUs 48 / 80
Shaders Unified: 1280
Current Clocks (MHz)
GPU 227.5
Memory 202.5
Video 544.0
Memory Modules
[#0] Corsair CMK32GX4M2A2666C16
Size 16 GB
Clock 1333 MHz
ECC N
Type DDR4-2666 / PC4-21300 DDR4 SDRAM UDIMM
Freq CL RCD RP RAS RC Ext. V
1066 15 15 15 36 50 - 1.20
1000.0 14 14 14 33 47 - 1.20
933.3 13 13 13 31 44 - 1.20
866.7 12 12 12 29 41 - 1.20
800.0 11 11 11 27 38 - 1.20
733.3 10 10 10 25 35 - 1.20
666.7 9 9 9 22 31 - 1.20
600.0 9 9 9 20 28 - 1.20
1333 16 18 18 35 53 XMP 1.20
Memory
Size 64 GB
Type DDR4 SDRAM
Clock 1077.1 MHz = 10.67 x 101.0 MHz
Mode Dual-Channel
CR 2T
Timing 15 - 15 - 15 - 36 tRC tRFC 374
Operating System
Legacy Boot
Microsoft Windows 10 Professional (x64) Build 14393.576 (RS1)

Memory training

- MRC – Memory reference code
- Q: How to run code (MRC) when memory is not yet available?
- A: Use CAR – ‘Cache as RAM’

Memory controller

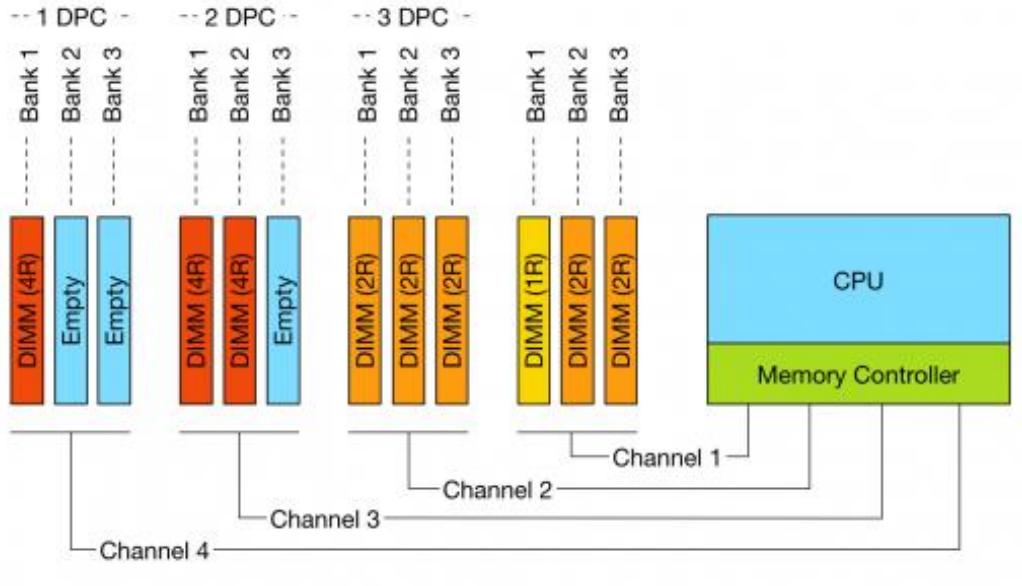
- In the past: dedicated chip (integrated in north bridge)
- Present: integrated into CPU-package
  - Called IMC (Integrated Memory Controller)
- Responsible for refreshing memory cells
- Takes the memory address as an input and fetches/writes data from/to main memory (DRAM).
- Usually integrated with MMU (memory management unit)

Multi-channel memory architecture

- MC has to support additional channels
- Requires specific memory configuration
  - At least two modules for Dual-Channel
    - Three for Triple-Channel, four for Quad-Channel
  - Some implementations allow for ‘Flexible mode’
    - different modules’ capacity
- Dual/Triple/Quad-Channel interleaved
  - spreads the data among different modules
  - allows for greater speeds
- DDR5 has additionally introduced sub-channels

Multi-Channel, multi-dimm

- DPC
  - DIMMs per channel
- MC can use only one DIMM in a channel at the same time



Attacks/mitigations

- Cold-boot attacks
- Rowhammer
  - Memory scrambling
  - Intel's Total Memory Encryption
  - Memory scrubbing
  - ECC

Memory timings

- CL – CAS Latency
  - CAS = Column Address Strobe
- T_{RCD} - **R**ow Address to **C**olumn Address **D**elay
- T_{RP} - **R**ow **P**recharge Time
- T_{RAS} - Row Active Time (**R**ow **A**ddress **S**trobe)
- Usually presented in ‘number of clock-cycles’

Memory timings

- Format: XX-XX-XX-XX
  - 1) CL
  - 2) tRCD
  - 3) tRP
  - 4) tRAS
  - Some can be ommited
- CL=11, tRCD=12
  - F3 is manufacturer specific info
- Note: 12800S => 1600Mhz

Combining Memory modules

- To make word larger
- To add more address lines

Additional materials

- https://www.atpinc.com/blog/DDR5-dimm-types-rdimm-vs-udimm-for-server-platform
- https://frankdenneman.nl/2015/02/18/memory-tech-primer-memory-subsystem-organization/
- https://www.youtube.com/watch?v=7J7X7aZvMXQ